INSTITUTO FEDERAL DE SANTA CATARINA
Departamento Acadêmico de Eletrônica
Pós-Graduação em Desenvolvimentos de Produtos Eletrônicos
Conversores Estáticos e Fontes Chaveadas

Avaliação Final

Conversores CA-CC-CC - Flyback

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SUMARIO

LISTA DE FIGURAS

1. INTRODUÇÃO

O objetivo desta avaliação é projetar um Conversor Flyback, projetando o circuito retificador de entrada com filtro capacitivo, o transformador, os componentes do estágio de potência, o comando e o controle do conversor, simular o circuito no PSim utilizando os dados encontrados e analisar os dados obtidos através da simulação com os dados teóricos.

Para os cálculos serão utilizadas as metodologias apresentadas em sala de aula com a ajuda do *software* Mathcad.

O Conversor Flyback tem a finalidade de transformar a tensão alternada de 220 V da rede elétrica comercial em duas tensões contínuas independentes, uma de 15 V / 0,5 A e outra de 5 V / 1A.

A tensão da rede elétrica comercial entra em um circuito retificador com filtro capacitivo, que tem a finalidade de retificar a onda. Esta tensão retificada entra no na fonte chaveada, transformando-a nas duas tensões requeridas. Todos estes passos serão discriminados, simulados e descritos no decorrer deste relatório.

Os componentes listados podem não ser as melhores escolhas, porém, para efeitos de aprendizado, condizem com a realidade.

2. DESENVOLVIMENTO

2.1 Especificações do Projeto

Foram dadas as seguintes especificações para este circuito:

Vac Universal = 85V a 265V eficazes

Vacmin := 85 V Vacmax := 265 V Fr := 60 Hz Vout1 := 15 V Iout1 := 0.5 A

Vout2 := 5 V Iout2 := 1 A ΔVoutret := 0.05 V (5%) Fcon := 50000 Hz

Vd := 1 V ΔVout := 0.01 V (1%) Voutaux := 15 V Ioutaux := 0.2 A

$$Vac := \frac{Vacmax + Vacmin}{2} \qquad \boxed{Vac = 175\ V}$$

$$\Delta Vac := \left(\frac{Vacmax \cdot 100}{Vac}\right) - 100 \qquad \boxed{\Delta Vac = 51.429\ \%}$$

2.1.1 Considerações preliminares para condições críticas

$\eta ret := 0.9$ Rendimento do retificador

$\eta con := 0.7$ Rendimento do conversor

2.1.1.1 Potências de saída

$$Pcon1 := Vout1 \cdot Iout1 \qquad \boxed{Pcon1 = 7.5\ W}$$

$$Pcon2 := Vout2 \cdot Iout2 \qquad \boxed{Pcon2 = 5\ W}$$

$$Pout1 := \frac{Pcon1}{\eta con} \qquad \boxed{Pout1 = 10.714\ W}$$

$$Pout2 := \frac{Pcon2}{\eta con} \qquad \boxed{Pout2 = 7.143 \quad W}$$

$$Pout := Pout1 + Pout2 \qquad \boxed{Pout = 17.857 \quad W}$$

$$Pin := \frac{Pout}{\eta ret} \qquad \boxed{Pin = 19.841 \quad W}$$

2.2 Diagrama de Blocos

Uma fonte chaveada pode ser representada pelo diagrama de blocos apresentado pela Figura 1 abaixo:

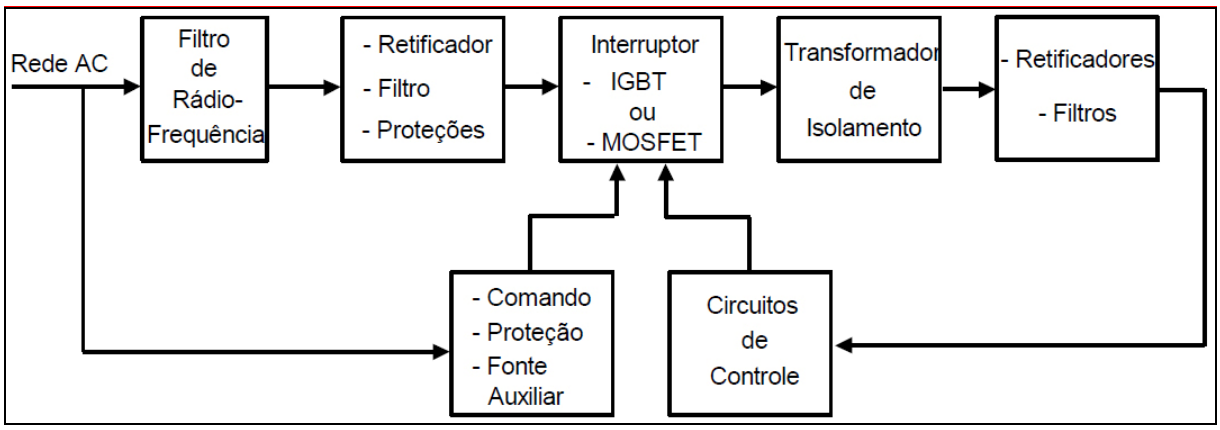


Figura 1 - Diagrama de Blocos

2.3 Descrição do funcionamento da Fonte Chaveada

A tensão alternada de 200 V é, primeiramente, transformada em tensão contínua através de um retificador de onda completa. Após esta transformação, ela é aplicada a um transformador Flyback, que converterá esta tensão em tensões de saída compatíveis com as especificadas pelo projeto, as quais são isoladas da rede elétrica por um transformador.

O conversor irá chavear a tensão gerando uma onda PWM, que utilizará uma realimentação em malha fechada para efetuar uma compensação das variações da rede elétrica, com o intuito de manter as tensões de saída constantes.

2.4 Projeto do Circuito Retificador, com filtro capacitivo

Foi projetado um circuito retificador com filtro capacitivo, mostrado pela Figura 2 abaixo:

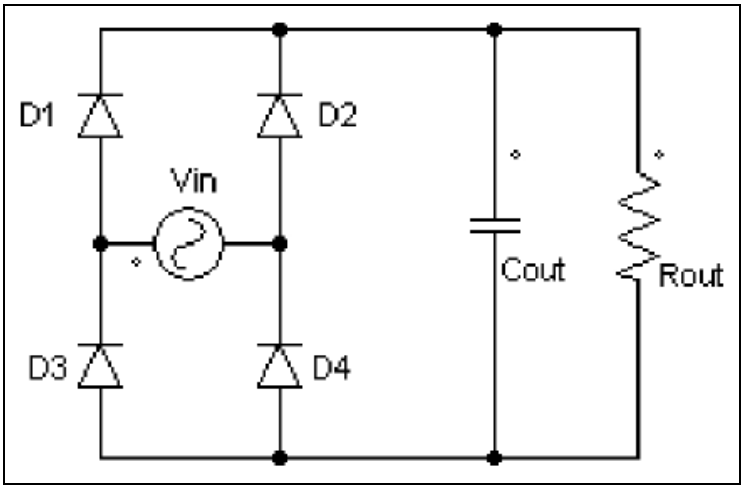


Figura 2 - Projeto do Circuito Retificador, com filtro capacitivo

2.4.1 Cálculo do capacitor de filtro

$Vcpkmin := \sqrt{2} \cdot Vacmin - Vd$ $\quad Vcpkmin = 119.208$ V

$Vcpkmax := \sqrt{2}\, Vacmax - Vd$ $\quad Vcpkmax = 373.767$ V

$Vcmin := (1 - \Delta Voutret) \cdot Vcpkmin$ $\quad Vcmin = 113.248$ V

$\Delta Vc := Vcpkmin - Vcmin$ $\quad \Delta Vc = 5.96$ V

$$Ccalc := \frac{Pin}{Fr \cdot \left(Vcpkmin^2 - Vcmin^2\right)} \qquad Ccalc = 2.387 \times 10^{-4}\ F$$

Valor comercial mais próximo do calculado: $Cret := 270 \cdot 10^{-6}$ F

$$Vcmedmin := \left(1 - \frac{\Delta Voutret}{2}\right) \cdot Vcpkmin \qquad Vcmedmin = 116.228\ V$$

$$Vcmedmax := \left(1 - \frac{\Delta Voutret}{2}\right) \cdot Vcpkmax \qquad Vcmedmax = 364.422 \ V$$

Conforme cálculos, será utilizado um capacitor de 270µF de 400V.

2.4.2 Cálculo dos diodos retificadores

$$tc := \frac{acos\left(\frac{Vcmin}{Vcpkmin}\right)}{2 \cdot \pi \cdot Fr} \qquad tc = 8.424 \times 10^{-4} \ s$$

$$Ipkretcalc := \frac{(Cret \cdot \Delta Voutret \cdot Vcpkmin)}{tc} \qquad Ipkretcalc = 1.91 \ A$$

De acordo com Ivo Barbi em **Eletrônica de Potência: Projeto de Fontes Chaveadas**, deve-se considerar uma Corrente de Pico com o dobro da amplitude, portanto:

$$Ipkret := 2 \cdot Ipkretcalc \qquad Ipkret = 3.821 \ A$$

$$Iefret := Ipkretcalc \cdot \sqrt{2 \cdot tc \cdot Fr - (2 \cdot tc \cdot Fr)^2} \qquad Iefret = 0.576 \ A$$

$$Icmed := \frac{Pin}{Vcmin} \qquad Icmed = 0.175 \ V$$

$$Icef := \sqrt{Iefret^2 + Icmed^2} \qquad Icef = 0.602 \ A$$

$$Idpk := Ipkret \qquad Idpk = 3.821 \ A$$

$$Idef := Idpk \cdot \sqrt{tc \cdot Fr} \qquad Idef = 0.859 \ A$$

$$Idmed := \frac{Pin}{2 \cdot Vcmin} \qquad Idmed = 0.088 \ A$$

$$Vdmax := \sqrt{2} \cdot Vacmax \qquad Vdmax = 374.767 \ V$$

Conforme cálculos, serão utilizados diodos de 1A / 400V para compor a ponte retificadora, cujo *datasheet* está disponível para consulta no Anexo 1.

2.5 Projeto do Transformador

2.5.1 Considerações iniciais

$Dmax := 0.4$ $\quad Jmax := 400\ \frac{A}{cm^2}$ $\quad \Delta B := 0.25\ T$ $\quad \mu o := 4\cdot\pi\cdot 10^{-7}\ \frac{H}{m}$

$Kp := 0.5$ $\quad Kw := 0.4$ $\quad Voutaux := 15\ V$ $\quad Ioutaux := 0.2\ A$

2.5.2 Escolha do Núcleo

$$AeAw := \frac{1.1\cdot Pout\cdot 10^4}{Kp\cdot Kw\cdot Jmax\Delta B\cdot Fcon} \qquad \boxed{AeAw = 0.196\ \ cm^4}$$

De acordo com a tabela apresentada pela Figura 3 abaixo, o núcleo deste Transformador deverá ser o E-30/7, pois possui o AeAw ligeiramente superior ao calculado.

NÚCLEOS DE FERRITE TIPO E

Tabela 2

Núcleo	A_e (cm^2)	A_w (cm^2)	l_e (cm)	l_t (cm)	v_e(cm^3)	A_eA_w (cm^4)
E-20	0,312	0,26	4,28	3,8	1,34	0,08
E-30/7	0,60	0,80	6,7	5,6	4,00	0,48
E-30/14	1,20	0,85	6,7	6,7	8,00	1,02
E-42/15	1,81	1,57	9,7	8,7	17,10	2,84
E-42/20	2,40	1,57	9,7	10,5	23,30	3,77
E-55	3,54	2,50	1,2	11,6	42,50	8,85

Material: IP6
Temperatura Curie: > 160°C

A_e - área de perna central;
A_w - área da janela do carretel;
l_e - comprimento magnético;
l_t - comprimento médio de um espira;
v_e - volume de ferrite;
B_{sat} - 0,3 T (para 85°C);
μ_o = 1 (CGS) - permeabilidade do ar;
= $4\pi\cdot 10^{-7}$ (SI);
μ_r = 3000 (CGS) para B = 100GAUSS (0,1T).

Figura 3 - Tabela de Nucleos de Ferrite Tipo E

Fonte: Livro Eletrônica de Potência: Projeto de Fontes Chaveadas, de Ivo Barbi

Como apresentado na tabela da Figura 3, os dados deste Núcleo são:

$Ae := 0.60\ cm^2$ área da perna central

$Aw := 0.80\ cm^2$ área da janela do carretel

$le := 6.7\ cm$ comprimento magnético

$lt := 5.6\ cm$ comprimento médio de uma espira

$Ve := 4\ cm^3$ volume do ferrite

$Ae \cdot Aw = 0.48\ cm^4$

2.5.3 Determinação do entreferro

$$\Delta W := \frac{Pout}{\eta con \cdot Fcon} \qquad \boxed{\Delta W = 5.102 \times 10^{-4}\ J}$$

$$\delta := \frac{2 \cdot \mu o \cdot \Delta W}{\Delta B^2 \cdot Ae \cdot 10^{-4}} \qquad \boxed{\delta = 3.419 \times 10^{-4}\ m}$$

$$lg := \frac{\delta}{2} \cdot 10^3 \qquad \boxed{lg = 0.171\ mm}$$

2.5.4 Número de espiras do primário

$$Ipkp := \frac{2 \cdot Pout}{\eta con \cdot Vcmedmin Dmax} \qquad \boxed{Ipkp = 1.097\ A}$$

$$Np := ceil\left(\frac{\Delta B \cdot \delta}{\mu o \cdot Ipkp}\right) \qquad \boxed{Np = 62\ espiras}$$

2.5.5 Número de espiras do secundário

$$Ns1 := ceil\left[Np \cdot \frac{(Vout1 + Vd)}{Vacmin} \cdot \frac{(1 - Dmax)}{Dmax}\right] \qquad \boxed{Ns1 = 18\ espiras}$$

$$Ns2 := ceil\left[Np \cdot \frac{(Vout2 + Vd)}{Vacmin} \cdot \frac{(1 - Dmax)}{Dmax}\right] \qquad \boxed{Ns2 = 7\ espiras}$$

2.5.6 Cálculo das correntes envolvidas

$$Iefp := Ipkp \cdot \sqrt{\frac{Dmax}{3}} \qquad Iefp = 0.401\ A$$

Corrente eficaz no primário do transformador

$$Ipks1 := Ipkp \cdot \left(\frac{Np}{Ns1}\right) \qquad \boxed{Ipks1 = 3.78\ A}$$

Corrente de pico na primeira saída do transformador

$$Iefs1 := Ipks1 \cdot \sqrt{\frac{1 - Dmax}{Fcon} \cdot \frac{Fcon}{3}} \qquad \boxed{Iefs1 = 1.69\ A}$$

Corrente eficaz na primeira saída do transformador

$$Imeds1 := \frac{Pout1}{Vout1} \qquad \boxed{Imeds1 = 0.714\ A}$$

Corrente média na primeira saída do transformador

$$Ipks2 := Ipkp \cdot \left(\frac{Np}{Ns2}\right) \qquad \boxed{Ipks2 = 9.72\ A}$$

Corrente de pico na segunda saída do transformador

$$Iefs2 := Ipks2 \cdot \sqrt{\frac{1 - Dmax}{Fcon} \cdot \frac{Fcon}{3}} \qquad \boxed{Iefs2 = 4.347\ A}$$

Corrente eficaz na segunda saída do transformador

$$Imeds2 := \frac{Pout2}{Vout2} \qquad \boxed{Imeds2 = 1.429\ A}$$

Corrente média na segunda saída do transformador

2.5.7 Cálculo da profundidade de penetração

A profundidade de penetração deve ser duplicada por 2 para que o cálculo seja para o diâmetro do condutor.

$$\Delta := 2 \cdot \left(\frac{7.5}{\sqrt{Fcon}}\right) \qquad \boxed{\Delta = 0.067\ cm}$$

De acordo com a tabela apresentada pela Figura 4 abaixo, o fio utilizado será o de espessura 22 AWG.

TABELA DE FIOS ESMALTADOS

Tabela 3

AWG	Diâmetro Cobre (cm)	Área Cobre (cm^2)	Diâmetro Isolamento (cm)	Área Isolamento (cm^2)	OHMS/CM 20 °C	OHMS/CM 100 °C	AMP. para 450A/cm^2
10	0,259	0,052620	0,273	0,058572	0,000033	0,000044	23,679
11	0,231	0,041729	0,244	0,046738	0,000041	0,000055	18,778
12	0,205	0,033092	0,218	0,037309	0,000052	0,000070	14,892
13	0,183	0,026243	0,195	0,029793	0,000066	0,000080	11,809
14	0,163	0,020811	0,174	0,023800	0,000083	0,000111	9,365
15	0,145	0,016504	0,156	0,019021	0,000104	0,000140	7,427
16	0,129	0,013088	0,139	0,015207	0,000132	0,000176	5,890
17	0,115	0,010379	0,124	0,012164	0,000166	0,000222	4,671
18	0,102	0,008231	0,111	0,009735	0,000209	0,000280	3,704
19	0,091	0,006527	0,100	0,007794	0,000264	0,000353	2,937
20	0,081	0,005176	0,089	0,006244	0,000333	0,000445	2,329
21	0,072	0,004105	0,080	0,005004	0,000420	0,000561	1,847
22	0,064	0,003255	0,071	0,004013	0,000530	0,000708	1,465
23	0,057	0,002582	0,064	0,003221	0,000668	0,000892	1,162
24	0,051	0,002047	0,057	0,002586	0,000842	0,001125	0,921
25	0,045	0,001624	0,051	0,002078	0,001062	0,001419	0,731
26	0,040	0,001287	0,046	0,001671	0,001339	0,001789	0,579
27	0,036	0,001021	0,041	0,001344	0,001689	0,002256	0,459

Figura 4 - Tabela de Fios Esmaltados

Fonte: Livro Eletrônica de Potência: Projeto de Fontes Chaveadas, de Ivo Barbi

Como apresentado na tabela da Figura 4, os dados deste fio são:

$A22 := 0.00325$ cm^2 $\quad \rho 22 := 0.00070$ $\frac{\Omega}{cm}$ $\quad S22 := 0.00401$ cm^2

2.5.8 Área dos condutores do primário do transformador

$$Sp := \frac{Iefp}{Jmax} \qquad \boxed{Sp = 1.002 \times 10^{-3}\ cm^2}$$

De acordo com a tabela da Figura 4, o fio escolhido para o primário do transformador é 25 AWG.

Os dados deste fio são:

$A25 := 0.00162$ cm^2 $\quad \rho 25 := 0.00141$ $\frac{\Omega}{cm}$ $\quad S25 := 0.00207$ cm^2

2.5.9 Área dos condutores dos dois secundários do transformador

2.5.9.1 Cálculos referentes ao primeiro secundário do transformador

$$Ss1 := \frac{Iefs1}{Jmax} \qquad \boxed{Ss1 = 4.226 \times 10^{-3}\ cm^2}$$

De acordo com a tabela da Figura 4, deveria ser utilizado um fio de 21 AWG, mas como este fio é mais espesso que o determinado pela profundidade de penetração, será utilizado mais de um fio em paralelo, de outra bitola.

$$Nfios1calc := \frac{Ss1}{A22} \qquad \boxed{Nfios1calc = 1.298}$$

Para que se tenha um maior aproveitamento do fio, serão utilizados 2 fios em paralelo do AWG 24 – determinado pela tabela da Figura 4 –, pois: $A24 := 0.00204'\ cm^2$

$$Nfios1calc24 := \frac{Ss1}{A24} \qquad Nfios1calc24 = 2.065$$. Arredondando, $\boxed{Nfios1 := 2}$, do Fio 24 AWG.

Os dados deste fio são:

$$A24 := 0.00204'\ cm^2 \qquad \rho 24 := 0.00112\ \frac{\Omega}{cm} \qquad S24 := 0.00258(\ cm^2$$

2.5.9.2 Cálculos referentes ao segundo secundário do transformador

$$Ss2 := \frac{Iefs2}{Jmax} \qquad \boxed{Ss2 = 0.011\ cm^2}$$

De acordo com a tabela da Figura 4, deveria ser utilizado um fio de 19 AWG, mas como este fio é mais espesso que o determinado pela profundidade de penetração, será utilizado mais de um fio em paralelo, de outra bitola.

$$Nfios2calc := \frac{Ss2}{A22} \qquad Nfios2calc = 3.339$$, arredondando: $\boxed{Nfios2 := 4}$, do fio 22 AWG.

Os dados deste fio são:

$$A22 := 0.00325:\ cm^2 \qquad \rho 22 := 0.00070(\ \frac{\Omega}{cm} \qquad S22 := 0.00401:\ cm^2$$

2.5.10 Cálculo das perdas no transformador

2.5.10.1 No primário

$Lfiop := lt \cdot Np$ $Lfiop = 347.2\ cm$ Comprimento do fio

$Vfiop := A25 \cdot Lfiop$ $Vfiop = 0.564\ cm^3$ Volume

$Rfiop := Np \cdot \rho 25 \cdot lt$ $Rfiop = 0.493\ \Omega$ Resistência do condutor

$Pp := Rfiop \cdot Iefp^2$ $Pp = 0.079\ W$ Perdas no condutor do primário

2.5.10.2 Na primeira saída do secundário

$Lfios1 := lt \cdot Ns1 \cdot Nfios1$ $Lfios1 = 201.6\ cm$ Comprimento do fio

$Vfios1 := A24 \cdot Lfios1$ $Vfios1 = 0.413\ cm^3$ Volume

$Rfios1 := \frac{Ns1 \cdot \rho 24 \cdot lt}{Nfios1}$ $Rfios1 = 0.057\ \Omega$ Resistência do condutor

$Ps1 := Rfios1 \cdot Iefs1^2$ $Ps1 = 0.162\ W$ Perdas no condutor do primário

2.5.10.3 Na segunda saída do secundário

$Lfios2 := lt \cdot Ns2 \cdot Nfios2$ $Lfios2 = 156.8\ cm$ Comprimento do fio

$Vfios2 := A22 \cdot Lfios2$ $Vfios2 = 0.51\ cm^3$ Volume

$Rfios2 := \frac{Ns2 \cdot \rho 22 \cdot lt}{Nfios2}$ $Rfios2 = 6.938 \times 10^{-3}\ \Omega$ Resistência do condutor

$Ps2 := Rfios2 \cdot Iefs2^2$ $Ps2 = 0.131\ W$ Perdas no condutor do primário

2.5.10.4 Perdas totais no transformador

$Ptc := Pp + Ps1 + Ps2$ $\boxed{Ptc = 0.372\ W}$ Perdas totais nos condutores

$Pesofio := 8.96 \cdot (Vfiop + Vfios1 + Vfios2)$ $\boxed{Pesofio = 13.323\ g}$

$K_H := 4 \cdot 10^{-5}$

$K_E := 4 \cdot 10^{-10}$

$Pnucleo := (\Delta B)^{2.4}\left(K_H \cdot Fcon + K_E \cdot Fcon^2\right) \cdot Ve$ $\boxed{Pnucleo = 0.431\ W}$

$Pt := Pnucleo + Ptc$ $\boxed{Pt = 0.803\ W}$

$Rt := 23 \cdot (Ae \cdot Aw)^{-0.37}$ $\boxed{Rt = 30.176\ ºC/W}$ Resistência térmica do transformador

$\Delta t := Pt \cdot Rt$ $\boxed{\Delta t = 24.232\ graus}$ Elevação de temperatura

2.5.11 Cálculo do fator de ocupação

$$Aw_{neces} := \frac{Np \cdot S25 + Ns1 \cdot S24 \cdot Nfios1 + Ns2 \cdot S22 \cdot Nfios2}{0.7}$$ $\boxed{Aw_{neces} = 0.478\ cm^2}$

$$K_{ocup} := \frac{Aw_{neces}}{Aw}$$ $\boxed{K_{ocup} = 0.597}$

Como o fator de ocupação é < 1, os condutores cabem no núcleo determinado previamente.

2.5.12 Determinação das indutâncias para simulação

$$Lmp := \frac{Np \cdot \Delta B \cdot Ae \cdot 10^{-4}}{Ipkp}$$ $\boxed{Lmp = 8.474 \times 10^{-4}\ H}$ Indutância presente no condutor do primário

$$Lms1 := \frac{Ns1 \cdot \Delta B \cdot Ae \cdot 10^{-4}}{Ipks1}$$ $Lms1 = 7.143 \times 10^{-5}$ H

Indutância presente no condutor do primeiro secundário

$$Lms2 := \frac{Ns2 \cdot \Delta B \cdot Ae \cdot 10^{-4}}{Ipks2}$$ $Lms2 = 1.08 \times 10^{-5}$ H

Indutância presente no condutor do segundo secundário

2.6 Projeto do Estágio de Potência

2.6.1 Cálculo dos tempos envolvidos

$$T := \frac{1}{Fcon}$$ $T = 2 \times 10^{-5}$ s

$Ton := Dmax \cdot T$ $Ton = 8 \times 10^{-6}$ s

$Toff := T - Ton$ $Toff = 1.2 \times 10^{-5}$ s

2.6.2 Determinação dos capacitores da saída

2.6.2.1 Determinação do capacitor da primeira saída

$\Delta Vout1 := Vout1 \cdot \Delta Voutret$ $\Delta Vout1 = 0.75$ V

$$Cout1calc := \frac{Imeds1 \cdot Dmax}{Fcon \cdot \Delta Vout1}$$ $Cout1calc = 7.619 \times 10^{-6}$ F

$Cout1 := 10 \cdot 10^{-6}$ F valor comercial mais próximo

$$RSE := \frac{\Delta Vout1}{Ipks1}$$ $RSE = 0.198$ Ω

Escolhe-se um capacitor de: 10 uF de 10 V, com RSE < 235 mΩ

2.6.2.2 Determinação do capacitor da segunda saída

$\Delta Vout2 := Vout2 \cdot \Delta Voutret$ $\Delta Vout2 = 0.25\ V$

$Cout2calc := \frac{Imeds2 \cdot Dmax}{Fcon \cdot \Delta Vout2}$ $Cout2calc = 4.571 \times 10^{-5}\ F$

$Cout2 := 47 \cdot 10^{-6}\ F$ valor comercial mais próximo

$RSE := \frac{\Delta Vout2}{Ipks1}$ $RSE = 0.066\ \Omega$

Conforme cálculos, será utilizado um capacitor de 47µF de 10V, com RSE < 78 mΩ

2.6.3 Determinação da chave

$Ipkch := Ipkp$ $Ipkch = 1.097\ A$ Corrente de pico na chave

$Iefch := \frac{Vacmin}{Fcon \cdot Lmp} \cdot \sqrt{\frac{Dmax^3}{3}}$ $Iefch = 0.293\ A$ Corrente eficaz na chave

$Imedch := \frac{Vacmin \cdot Dmax^2}{2 \cdot Fcon \cdot Lmp}$ $Imedch = 0.16\ A$ Corrente média na chave

$Vmaxch := Vacmax + (Vout1 + Vd) \cdot \frac{Np}{Ns1} + (Vout2 + Vd) \cdot \frac{Np}{Ns2}$ $Vmaxch = 373.254\ V$ Tensão máxima sobre a chave

Conforme cálculos, será utilizado o interruptor IRF 740D - 10A / 400V, cujo *datasheet* está disponível para consulta no Anexo 2.

Características da chave:

$Ta := 45\ ºC$ $RDSon := 1.1\ \Omega$ $Tr := 120 \cdot 10^{-9}\ s$

$RSjc := 1\ \frac{C}{W}$ $Tj := 150\ ºC$ $Tf := 140 \cdot 10^{-9}\ s$

2.6.3.1 Cálculos das perdas na chave

$Pchcond := RDSon \cdot Iefch^2$ $\boxed{Pchcond = 0.094\ W}$ Perdas na chave por condução

$Pchcom := \frac{Fcon}{2} \cdot (Tr + Tf) \cdot Ipkch \cdot Vmaxcl$ $\boxed{Pchcom = 2.663\ W}$ Perdas na chave por comutação

$Pcht := Pchcond + Pchcom$ $\boxed{Pcht = 2.757\ W}$ Perdas totais na chave

$Tcs := Tj - Pcht \cdot RSjc$ $\boxed{Tcs = 147.243\ ºC}$

$Rda := \frac{Tj - Ta}{Pcht} - 1$ $\boxed{Rda = 37.086\ \frac{ºC}{W}}$ Não se faz necessário o uso de dissipador

2.6.4 Determinação dos diodos de bloqueio

2.6.4.1 Determinação do diodo de bloqueio para saída a primeira saída

$To1 := \frac{Lms1 \cdot Ipks1}{Vout1 + Vd}$ $\boxed{To1 = 1.687 \times 10^{-5}\ s}$ Instante em que a corrente no diodo da saída 1 se anula

$Ipkd1 := Ipks1$ $\boxed{Ipkd1 = 3.78\ A}$ Corrente de pico no diodo da saída 1

$Iefd1 := Ipks1 \cdot \sqrt{\frac{To1}{3 \cdot T}}$ $\boxed{Iefd1 = 2.005\ A}$ Corrente eficaz no diodo da saída 1

$Imedd1 := \frac{Ipks1 \cdot To1}{2 \cdot T}$ $\boxed{Imedd1 = 1.595\ A}$ Corrente média no diodo da saída 1

$Vmaxd1 := Vout1 + Vacmax\frac{Ns1}{Np}$ $\boxed{Vmaxd1 = 91.935\ V}$ Tensão máxima sobre o diodo da saída 1

Conforme cálculos, será utilizado Diodo MUR810, que é para 100V / 8A, cujo *datasheet* está disponível para consulta no Anexo 3.

2.6.4.2 Determinação do diodo de bloqueio para saída a segunda saída

$To2 := \frac{Lms2 \cdot Ipks2}{Vout2 + Vd}$ $\boxed{To2 = 1.75 \times 10^{-5}\ s}$ Instante em que a corrente no diodo da saída 2 se anula

$Ipkd2 := Ipks2$ $\boxed{Ipkd2 = 9.72\ A}$ Corrente de pico no diodo da saída 2

$Iefd2 := Ipks2 \cdot \sqrt{\frac{To2}{3 \cdot T}}$ $\boxed{Iefd2 = 5.249\ A}$ Corrente eficaz no diodo da saída 2

$Imedd2 := \frac{Ipks2 \cdot To2}{2 \cdot T}$ $\boxed{Imedd2 = 4.253\ A}$ Corrente média no diodo da saída 2

$Vmaxd2 := Vout2 + Vacmax \cdot \frac{Ns2}{Np}$ $\boxed{Vmaxd2 = 34.919\ V}$	Tensão máxima sobre o diodo da saída 2

Conforme cálculos, será utilizado Diodo MUR805, que é para 50V / 8A, cujo *datasheet* está disponível para consulta no Anexo 3.

2.7 Escolha do circuito integrado dedicado para o comando e controle do conversor

Escolhido o circuito integrado UC 3524, cujo *datasheet* está disponível para consulta no Anexo 4.

2.8 Projeto dos Circuitos de Comando, Controle e auxiliares

$\boxed{Vref := 5\ V}$ Dado do CI escolhido

$\boxed{Rdiv1 := 100\ \Omega}$

$Rdiv2 := Rdiv1 \cdot \frac{(Voutaux - Vref)}{Vref}$ $\boxed{Rdiv2 = 2 \times 10^{3}\ \Omega}$

$Rout1 := \frac{Vout1}{Iout1}$ $\boxed{Rout1 = 30\ \Omega}$

$$Rout2 := \frac{Vout2}{Iout2} \qquad \boxed{Rout2 = 5\ \Omega}$$

$\boxed{Vs := 3.5\ V}$ Dado do UC 3524

2.8.1 Função de transferência do conversor Flyback em Malha Aberta

$$\omega := 10, 100.. 10^6\ \frac{rad}{s}$$

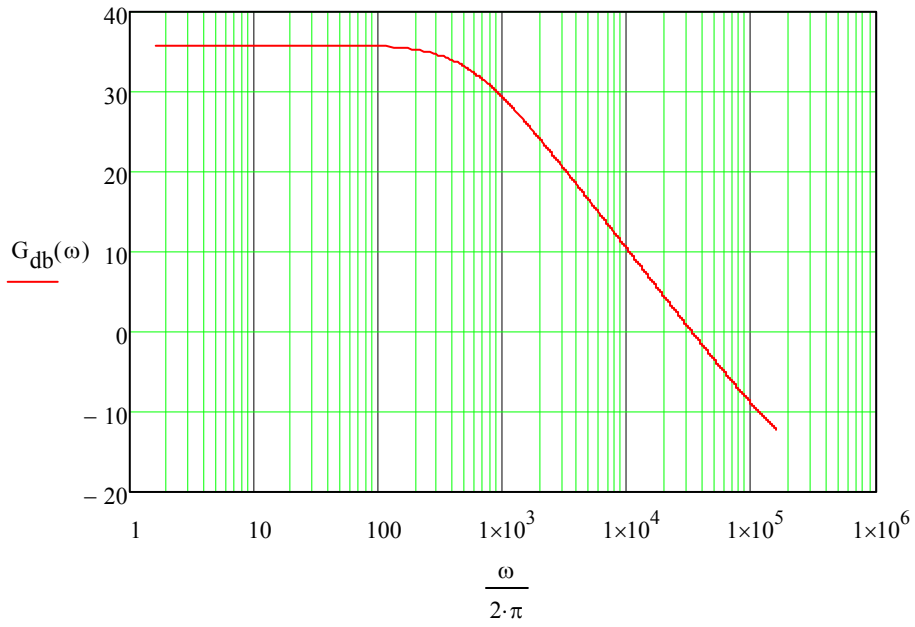
$$j := \sqrt{-1}$$

$$G(\omega) := \frac{Vcmedmax}{Vs \cdot \sqrt{\frac{2 \cdot Lmp \cdot Fcon}{Rout1}}} \cdot \frac{(1 + j \cdot \omega \cdot RSE \cdot Cout1)}{(1 + j \cdot \omega \cdot Rout1 \cdot Cout1)}$$

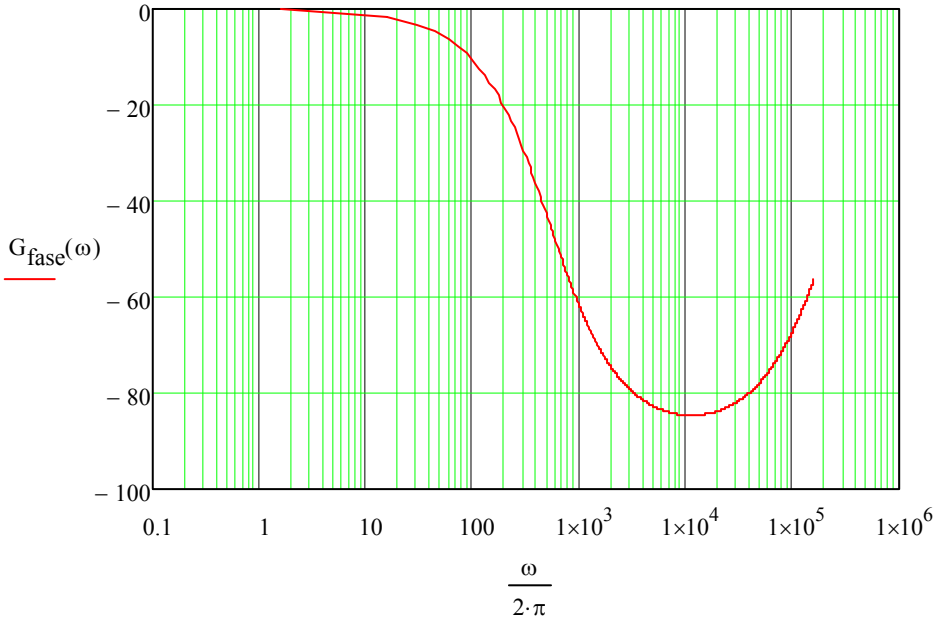
$$G_{db}(\omega) := 20 \cdot \log(|G(\omega)|)$$

$$G_{fase}(\omega) := \arg(G(\omega)) \cdot \frac{180}{\pi}$$

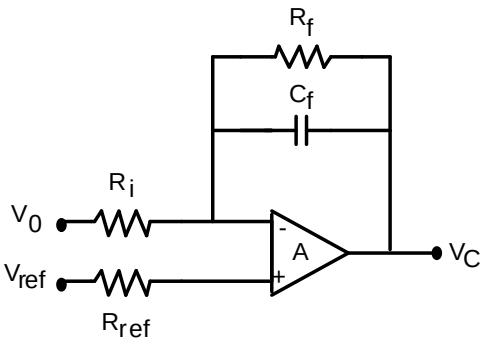
2.8.1.1 Diagramas de Bode da planta



$$G_{db}(0) = 35.841$$



2.8.2 Cálculo do controlador de 1 pólo



Ri := 1000 Ω

Ganho := 1

Rf := Ri·Ganho Rf = 1×10^{3} Ω

Fpolo := 100 Hz Posição do Polo

$$Cfcalc := \frac{1}{2\cdot\pi\cdot Rf\cdot Fpolo}$$

Cfcalc = 1.592×10^{-6} F

Cf := $1.8\cdot10^{-6}$ F valor comercial mais próximo

Conforme cálculos, será utilizado um capacitor de 1.8 uF de 10 V, com RSE < 78 mΩ.

$$Fcorte := \frac{Fcon}{100}$$

Fcorte = 500 Hz

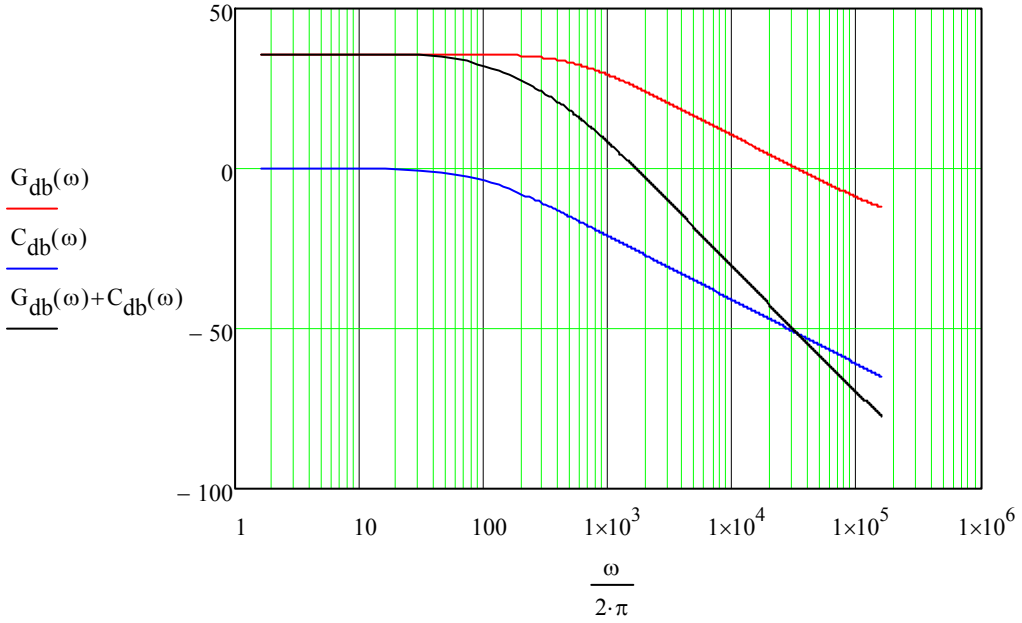
2.8.2.1 Função de transferência do controlador

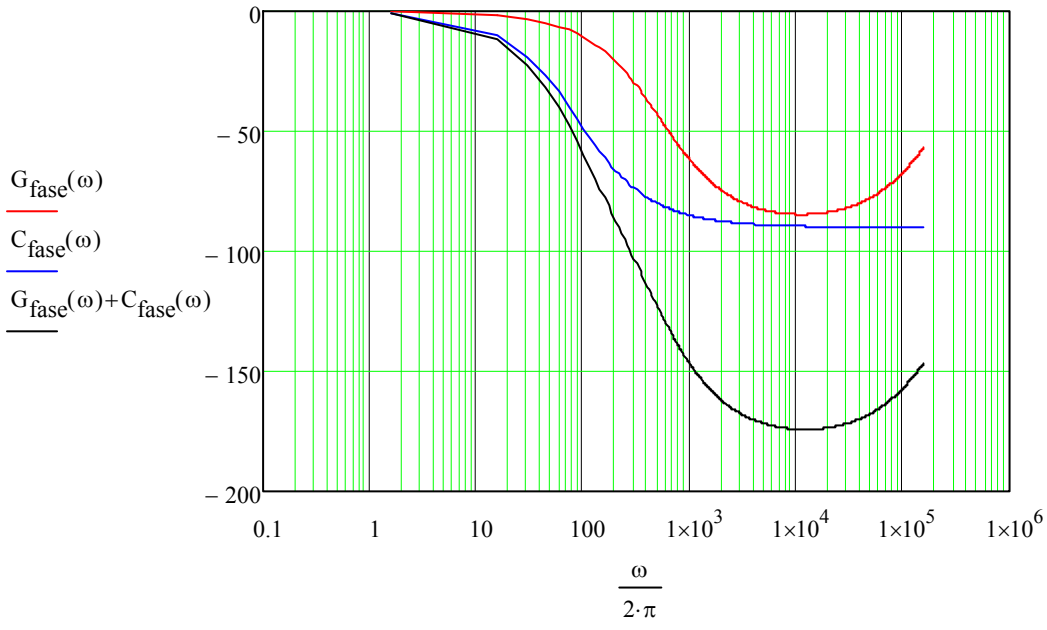
$$C(\omega) := \frac{Rf}{Ri} \cdot \frac{1}{(1 + j \cdot \omega \cdot Rf \cdot Cf)}$$

$$C_{db}(\omega) := 20 \cdot \log(|C(\omega)|)$$

$$C_{fase}(\omega) := \arg(C(\omega)) \cdot \frac{180}{\pi}$$

2.8.2.2 Diagrama de Bode do sistema





2.8.2.3 Margem de fase

$G_{fase}(2\cdot\pi\ Fcorte) = -43.185\ graus$

$C_{fase}(2\cdot\pi\ Fcorte) = -79.972\ graus$

$MF := 180 + \left(G_{fase}(2\cdot\pi\ Fcorte) + C_{fase}(2\cdot\pi\ Fcorte)\right)$ $MF = 56.844\ graus$

2.9 Projeto de Circuitos Auxiliares

2.9.1 Componentes auxiliares

$RT := 400\ \Omega$ Dado do UC 3524

$CT := 10\cdot10^{-9}\ F$

$IC := 0.1\ A$

$Ron := \frac{Voutaux}{IC}$ $Ron = 150\ \Omega$

Conforme cálculos, será um resistor de pulldown de 1000 Ω e um zener de 16 V / 0,5 W.

2.9.2 Fonte auxiliar para partida

$Vopartida := 12\ V$

$Rdiv3 := 1000\ \Omega$

$Rdiv4 := Rdiv3\cdot\frac{(Vcmedmax - Vopartida)}{Vopartida}$ $Rdiv4 = 2.937\times10^{4}\ \Omega$

$Idiv := \frac{Vcmedmax}{Rdiv3 + Rdiv4}$ $Idiv = 0.012\ A$

$PRdiv3 := Rdiv3 \cdot Idiv^2$ $\quad PRdiv3 = 0.144\ W$

$PRdiv4 := Rdiv4 \cdot Idiv^2$ $\quad PRdiv4 = 4.229\ W$

$Vopartidamin := \frac{Vcmedmin\,Rdiv3}{Rdiv3 + Rdiv4}$ $\quad Vopartidamin = 3.827\ V$

Conforme cálculos, será um capacitor de: 100 uF / 25 V e um Diodo Zener de 12 V de 1 W.

$I_{Zmax} := \frac{1}{12}$ $\quad I_{Zmax} = 0.083\ A$

$I_{Zmin} := 0.1 \cdot I_{Zmax}$ $\quad I_{Zmin} = 8.333 \times 10^{-3}\ A$

$Rsmax := \frac{Vcmedmax - Vopartida}{I_{Zmin}}$ $\quad Rsmax = 4.229 \times 10^{4}\ \Omega$

$Rsmin := \frac{Vcmedmin - Vopartida}{I_{Zmax}}$ $\quad Rsmin = 1.251 \times 10^{3}\ \Omega$

$Rs := 3300\ \Omega$

$P_{RS} := \frac{(Vcmedmax - Vopartida)^2}{Rs}$ $\quad P_{RS} = 3.764\ W$

2.9.2.1 Controle da corrente de partida

$Idmax := 30\ A$

$Rserie := \frac{\sqrt{2} \cdot Vacmax}{Idmax}$ $\quad Rserie = 12.492$

Será necessário usar termistor com resistência a frio maior que Rserie.

2.10 Lista de Componentes

Para a confecção da fonte chaveada será necessária a compra dos seguintes componentes.

2.10.1 Resistores

- 03 Resistores de 1kΩ;
- 01 Resistor de 2kΩ;
- 01 Resistor de 30Ω;
- 01 Resistor de 5Ω;
- 01 Resistor de 33kΩ;

2.10.2 Capacitores

- 01 Capacitor de 270μF / 400V;
- 01 Capacitor de 10μF / 10V com RSE < 235mΩ;
- 01 Capacitor de 47μF / 10V com RSE < 78mΩ;
- 01 Capacitor de 1,8 μF / 10 V com RSE < 78mΩ;
- 01 Capacitor de 100μF / 25V;

2.10.3 Diodos

- 04 Diodos de 1A / 400V;
- 01 Diodo de 100V / 8A, modelo MUR810;
- 01 Diodo de 50V / 8A, modelo MUR805;
- 01 Diodo Zener de 16 V / 0,5 W;
- 01 Diodo Zener de 12V / 1W;

2.10.4 Transformador

- 01 Transformador com 62 espiras no primário e dois secundários, de 18 e 07 espiras;
- 01 Núcleo E-30/7 de Ferrite para Transformador;

2.10.5 Fios

- 5,1 m de Fio 22 AWG;
- 2,1 m de Fio 24 AWG;

2.10.6 Chave

- 01 Chave de 10A / 400V, modelo IRF 740D;

2.10.7 Circuitos integrados

- 01 CI UC 3524;

2.11 Esquemático Completo

A Figura 5 abaixo, mostra o esquemático completo da fonte chaveada.

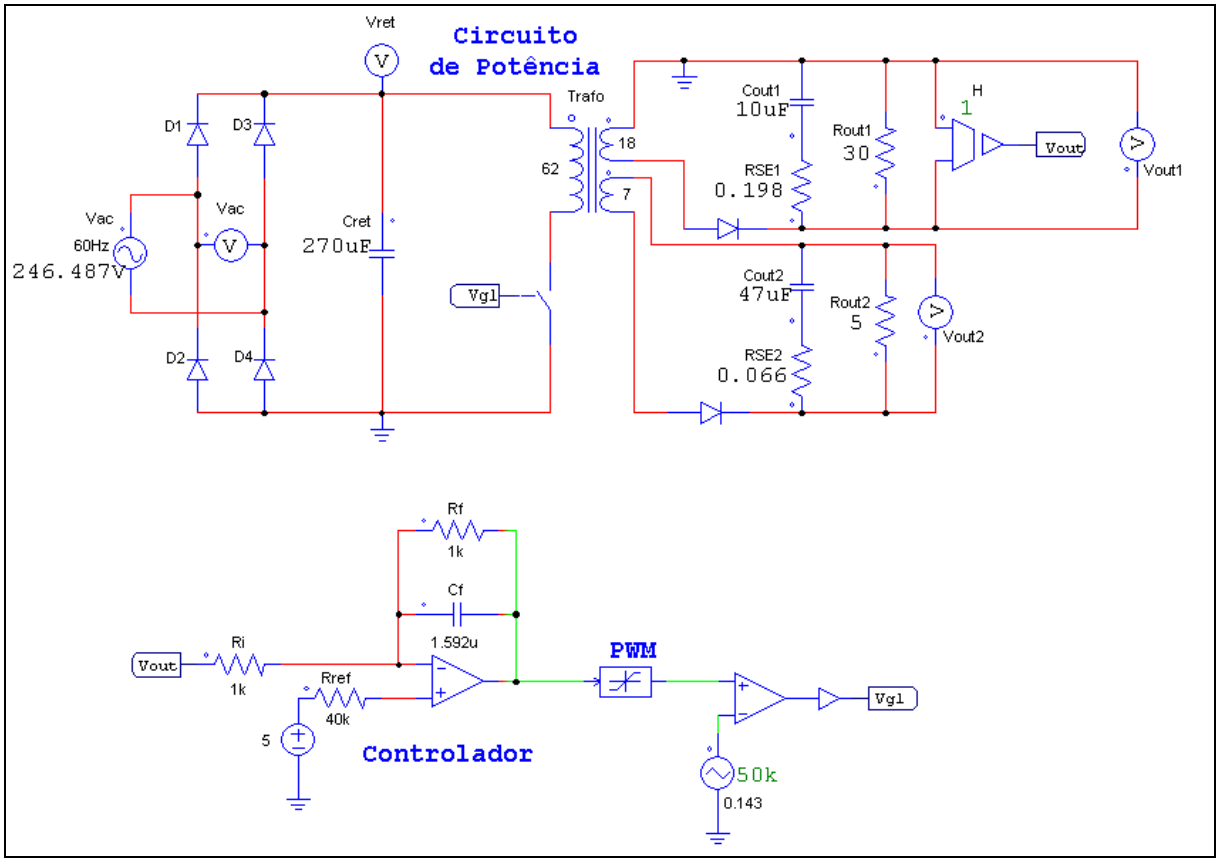


Figura 5 - Esquemático completo

2.12 Resultados da Simulação

2.12.1 Simulação em Malha Aberta

2.12.1.1 Com tensão mínima de entrada

A Figura 6 abaixo mostra o circuito para simulação com tensão mínima de entrada, em Malha Aberta.

Para obter valores próximos aos determinados, foi necessário alterar a razão cíclica para 0,3.

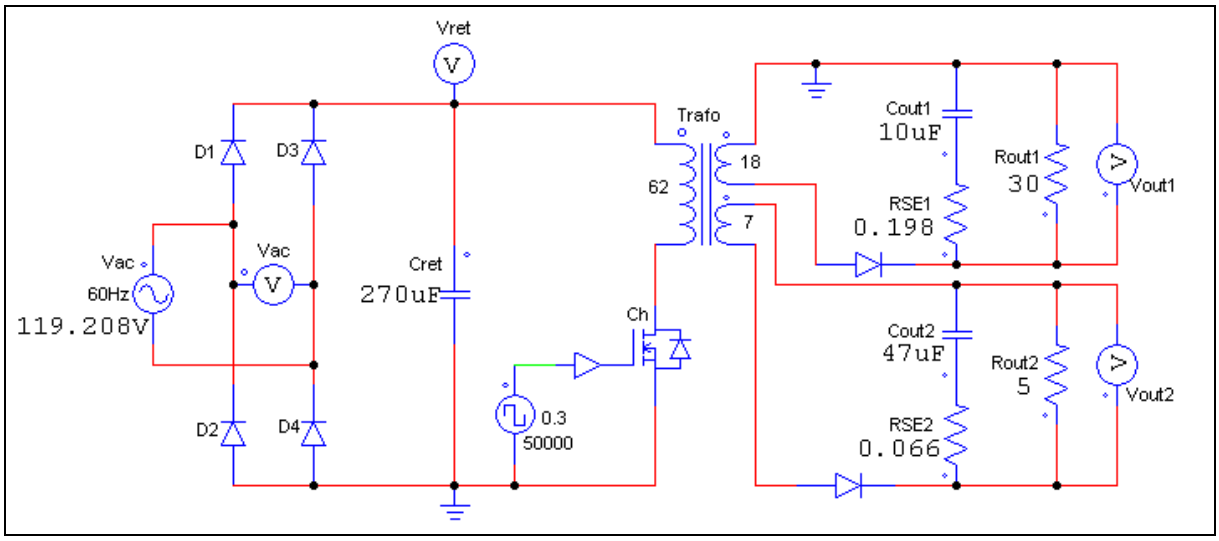


Figura 6 - Circuito para simulação com tensão mínima de entrada em Malha Aberta

A Figura 7 abaixo mostra as formas de onda da tensão de entrada e da tensão na saída do retificador em Malha Aberta.

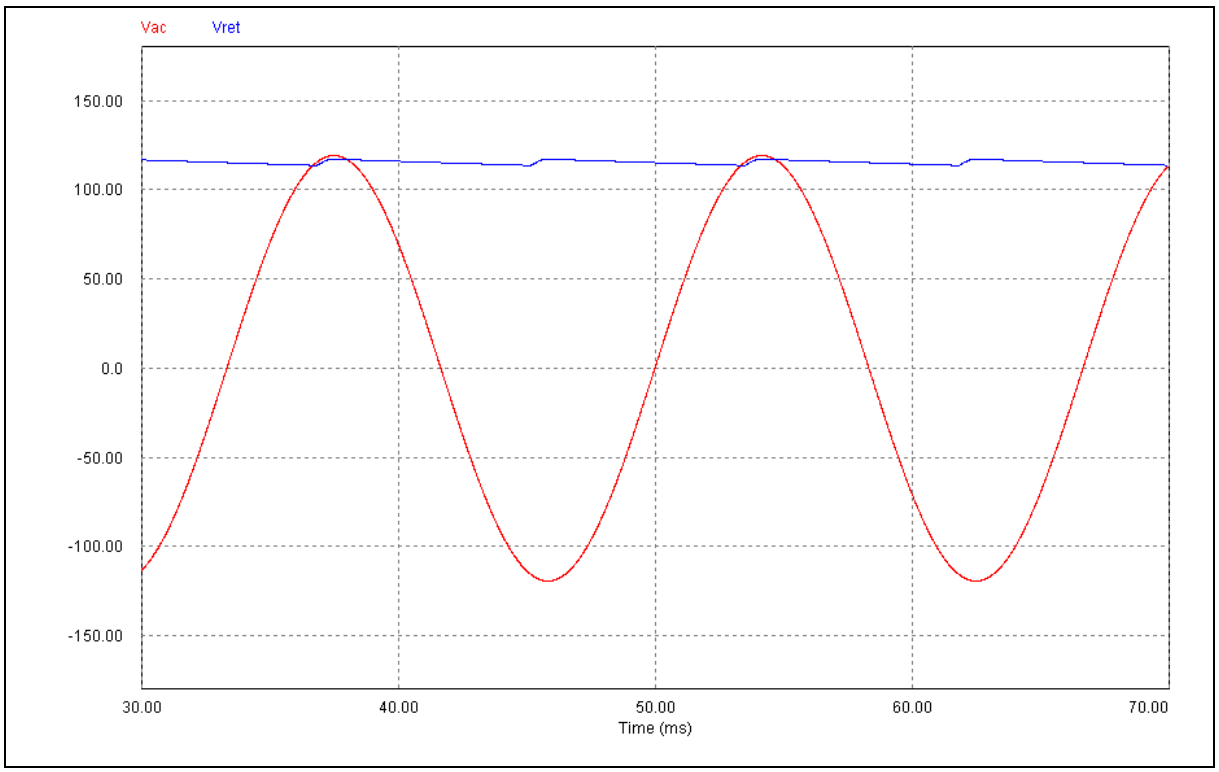


Figura 7 - Formas de onda da tensão de entrada e da tensão na saída do retificador com tensão mínima de entrada em Malha Aberta

A Figura 8 abaixo mostra o *ripple* da forma de onda da tensão na saída do retificador em Malha Aberta.

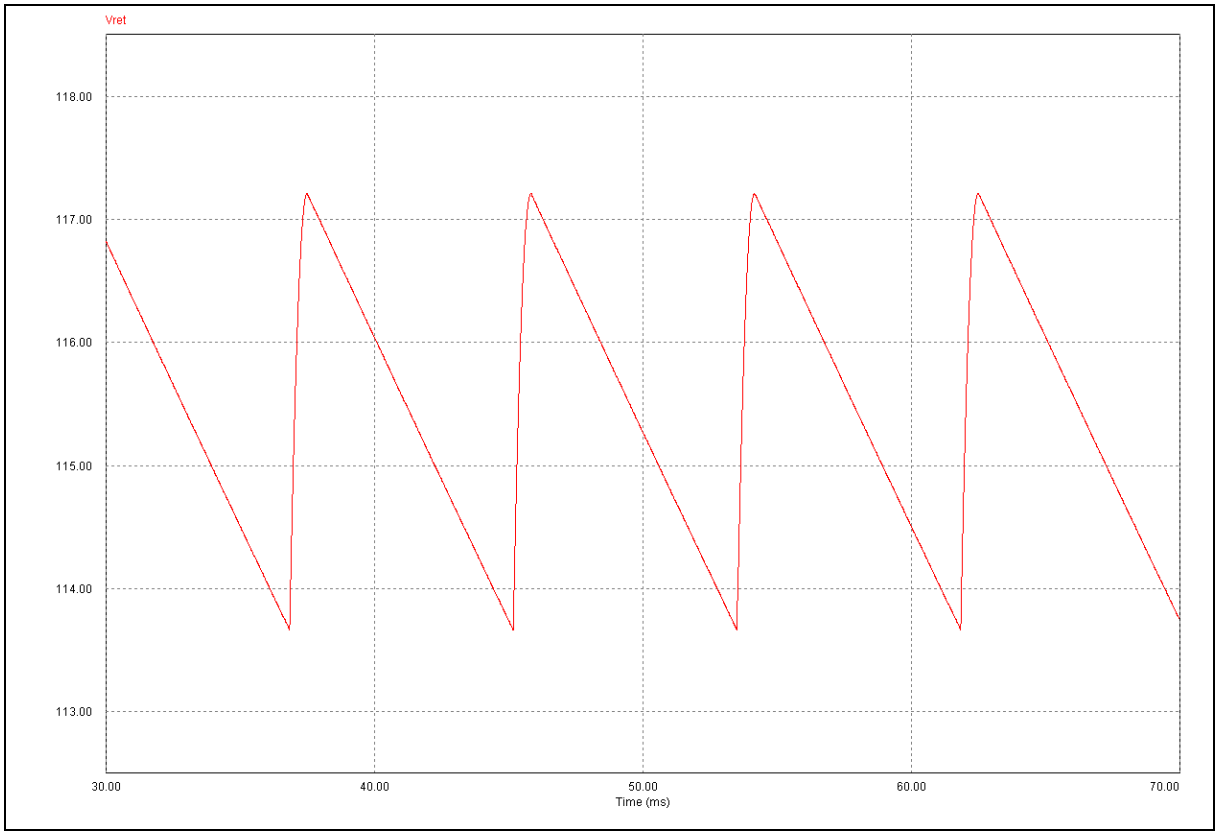


Figura 8 - *Ripple* da forma de onda da tensão na saída do retificador com tensão mínima de entrada em Malha Aberta

Vret máx = 117,208V

Vret min = 113,665V

Vret méd = 115,445V

A Figura 9 abaixo mostra, de forma ampliada, as formas de onda das correntes em dois diodos retificadores e da corrente na chave, com o circuito em Malha Aberta.

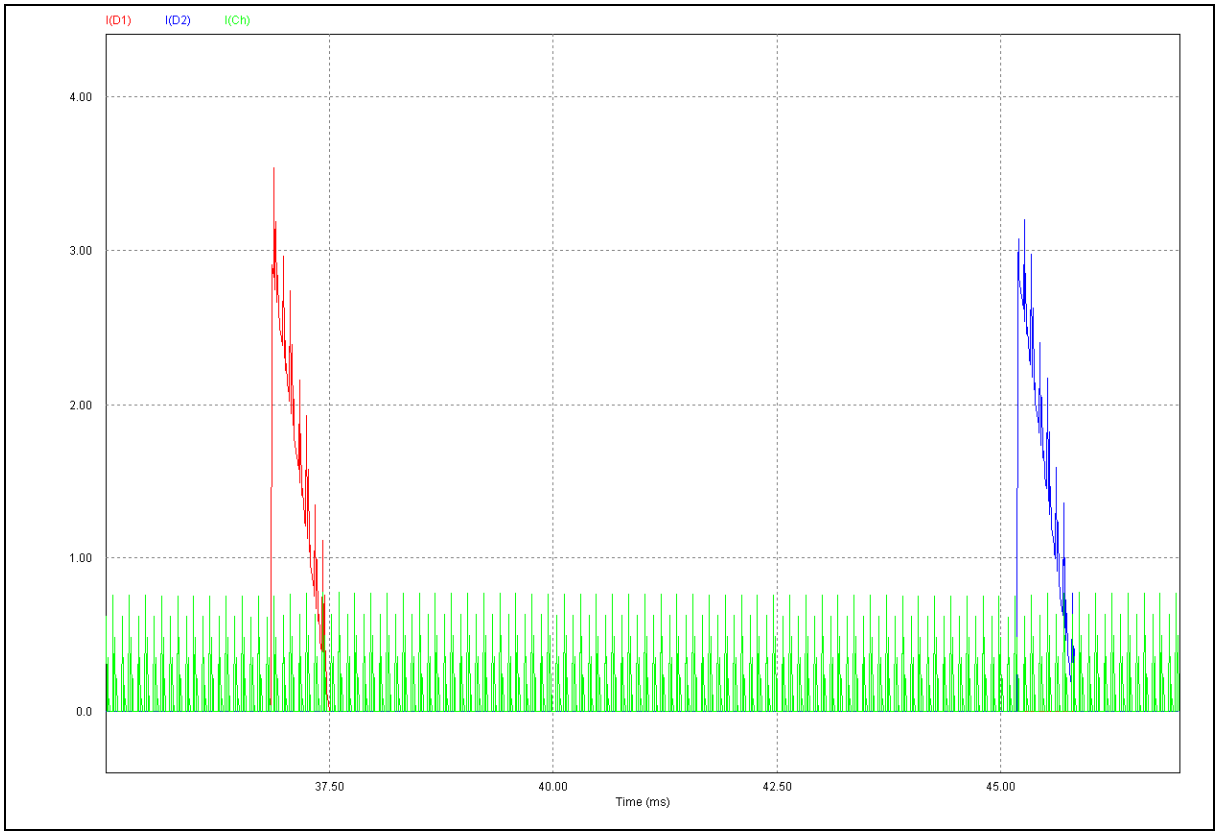


Figura 9 - Ampliação das formas de onda das correntes em dois diodos retificadores e da corrente na chave, com tensão mínima de entrada em Malha Aberta

Id1 pk = 3,535A

Id2 pk = 3,20159A

Ich pk = 0,772303A

Ich méd = 0,126862A

A Figura 10 abaixo mostra as formas de onda das tensões e correntes nas duas saídas, em Malha Aberta.

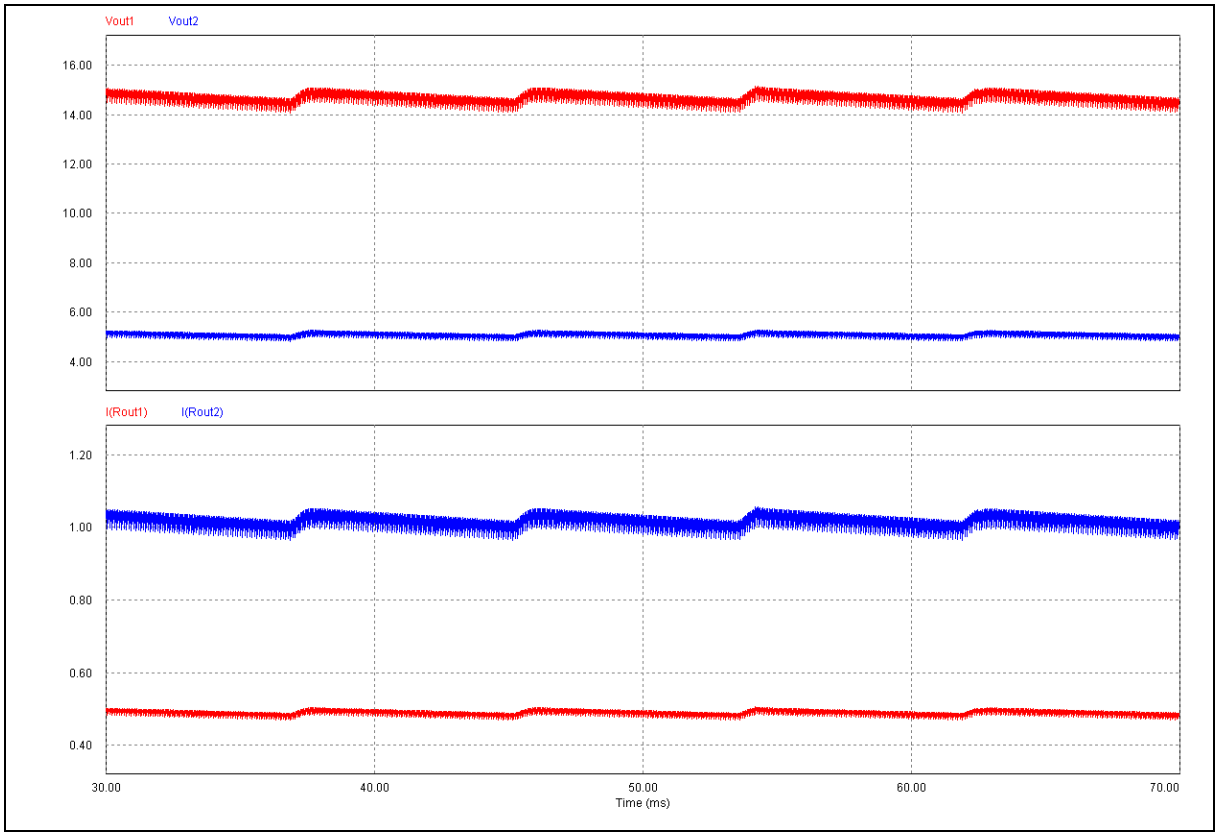


Figura 10 - Formas de onda das tensões e correntes nas duas saídas, com tensão mínima de entrada em Malha Aberta

Vout1 máx = 15,1572V

Vout1 min = 14,0823V

Vout1 méd = 14,67V

Vout2 máx = 5,28251V

Vout2 min = 4,8237V

Vout2 méd = 5,08114V

Iout1 máx = 0,505241A

Iout1 min = 0,469409A

Iout1 méd = 0,489001A

Iout2 máx = 1,0565A

Iout2 min = 0,964741A

Iout2 méd = 1,01623A

2.12.1.2 Com tensão máxima de entrada

A Figura 11 abaixo mostra o circuito para simulação com tensão máxima de entrada, em Malha Aberta.

Para obter valores próximos aos determinados, foi necessária alterar a razão cíclica para 0,094.

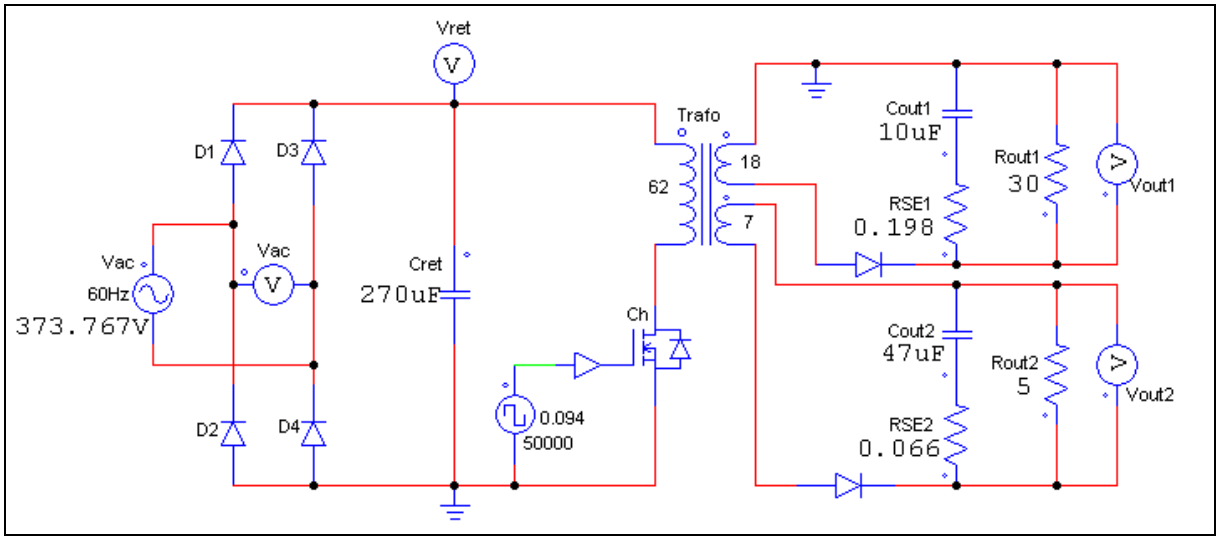


Figura 11 - Circuito para simulação com tensão máxima de entrada em Malha Aberta

A Figura 12 abaixo mostra as formas de onda da tensão de entrada e da tensão na saída do retificador em Malha Aberta.

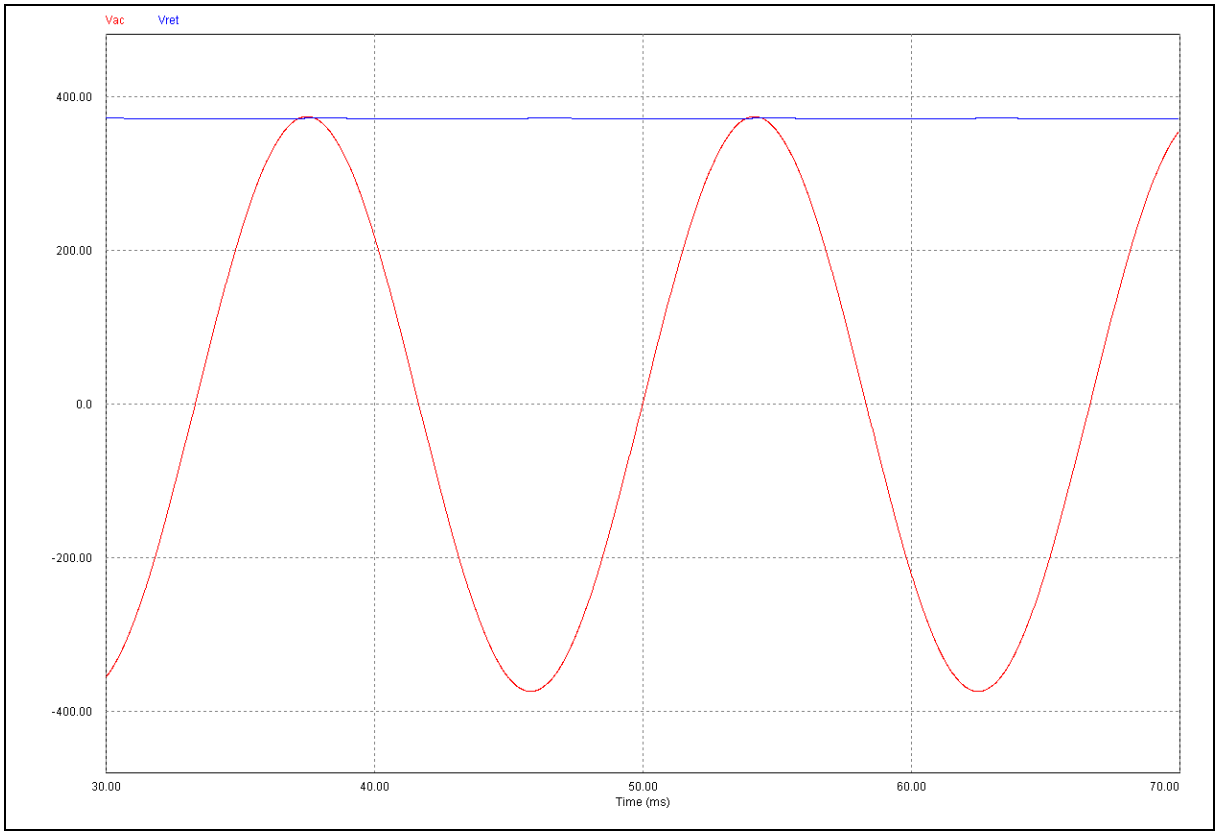


Figura 12 - Formas de onda da tensão de entrada e da tensão na saída do retificador com tensão máxima de entrada em Malha Aberta

A Figura 13 abaixo mostra o *ripple* da forma de onda da tensão na saída do retificador em Malha Aberta.

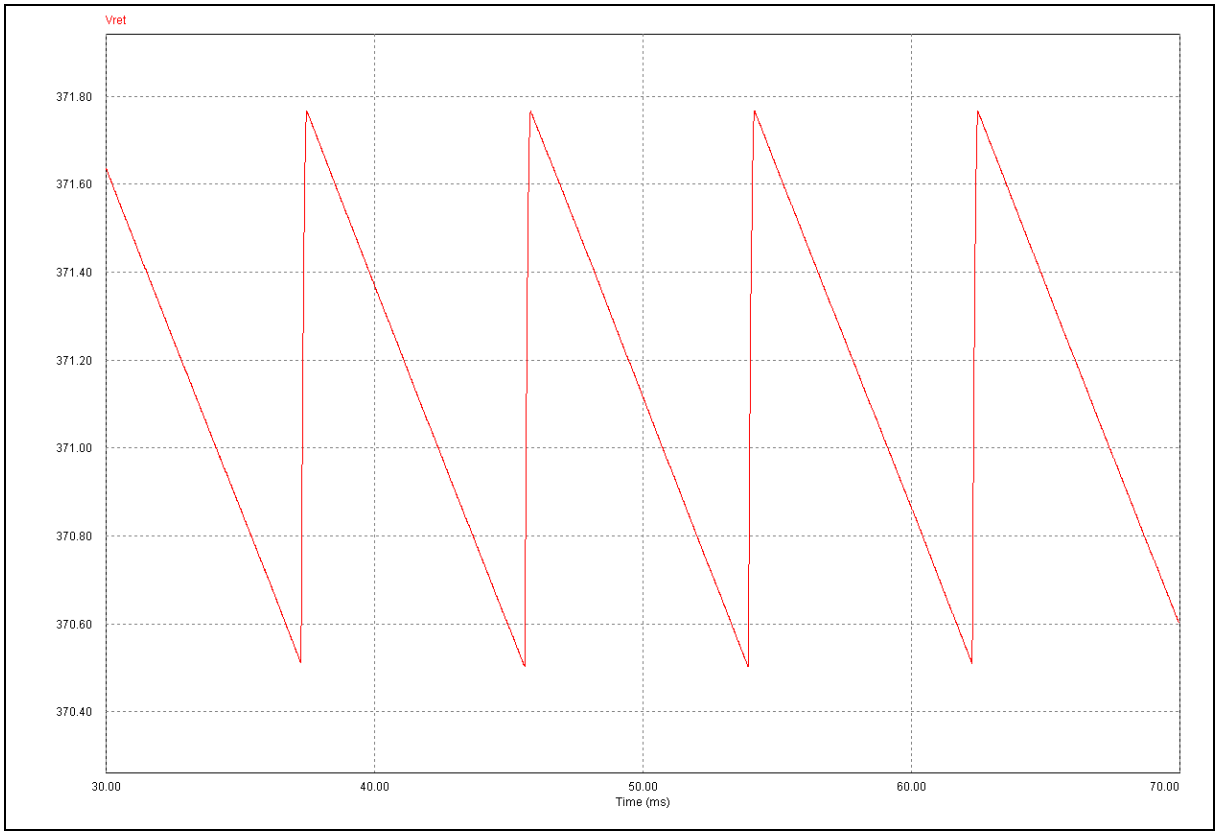


Figura 13 - *Ripple* da forma de onda da tensão na saída do retificador com tensão máxima de entrada em Malha Aberta

Vret máx = 371,767V

Vret min = 370,502V

Vret méd =371,137V

A Figura 14 abaixo mostra, de forma ampliada, as formas de onda das correntes em dois diodos retificadores e da corrente na chave, com o circuito em Malha Aberta.

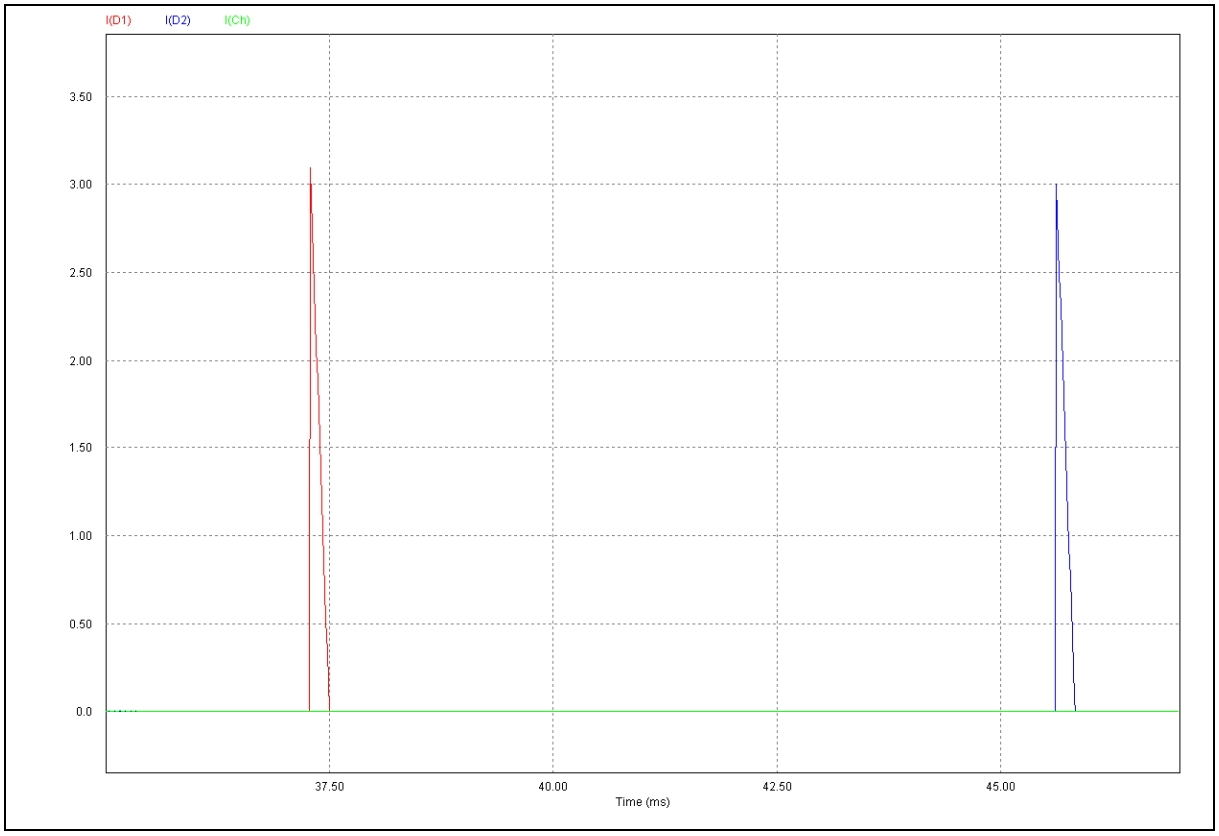


Figura 14 - Ampliação das formas de onda das correntes em dois diodos retificadores e da corrente na chave, com tensão máxima de entrada em Malha Aberta

Id1 pk = 3,09299A

Id2 pk = 3,00368A

A Figura 15 abaixo mostra as formas de onda das tensões e correntes nas duas saídas, em Malha Aberta.

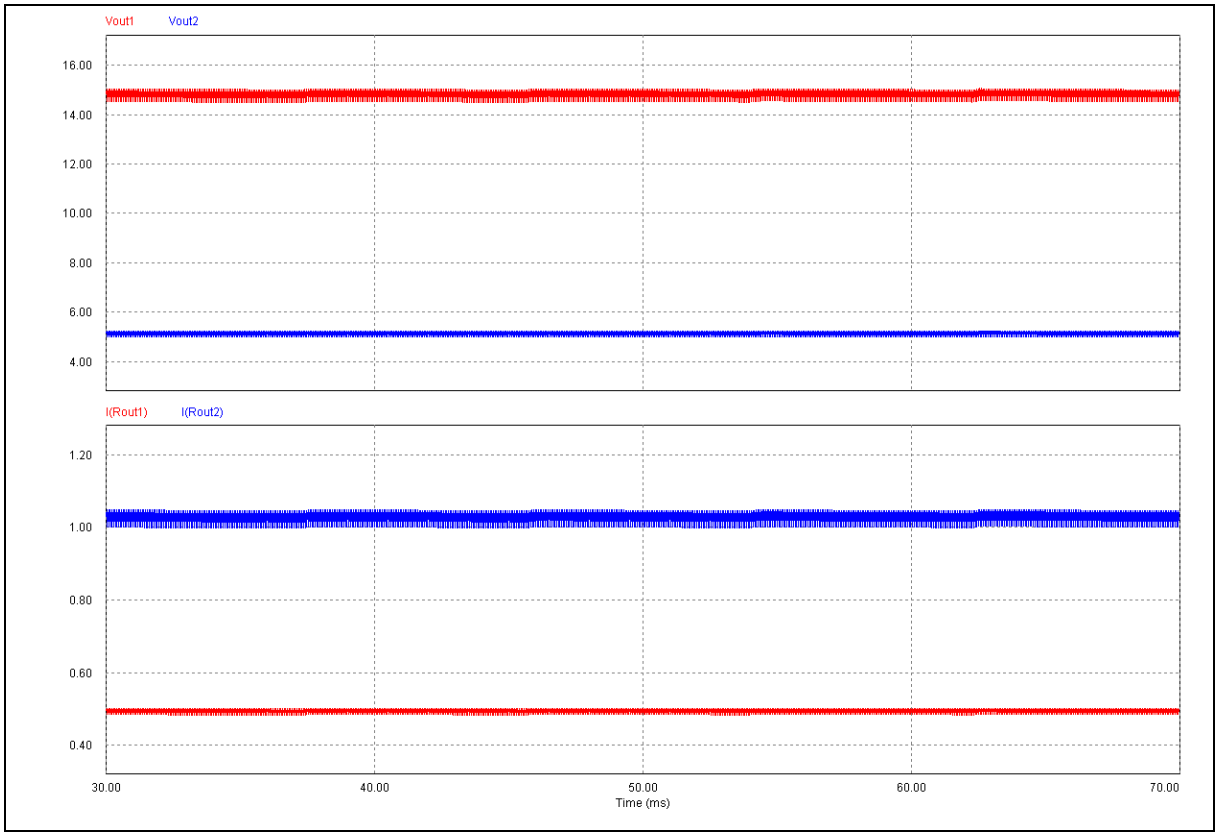


Figura 15 - Formas de onda das tensões e correntes nas duas saídas, com tensão máxima de entrada em Malha Aberta

Vout1 máx = 15,0612V

Vout1 min = 14,4934V

Vout1 méd = 14,8284V

Vout2 máx = 5,24536V

Vout2 min = 4,98722V

Vout2 méd = 5,14119V

Iout1 máx = 0,502042A

Iout1 min = 0,483114A

Iout1 méd = 0,49428A

Iout2 máx = 1,04907A

Iout2 min = 0,997444A

Iout2 méd = 1,02824A

2.12.1.3 Com tensão média de entrada

A Figura 16 abaixo mostra o circuito para simulação com tensão média de entrada, em Malha Aberta, para simular condições reais, e não extremas, da fonte.

Para obter valores próximos aos determinados, foi necessária alterar a razão cíclica para 0,143.

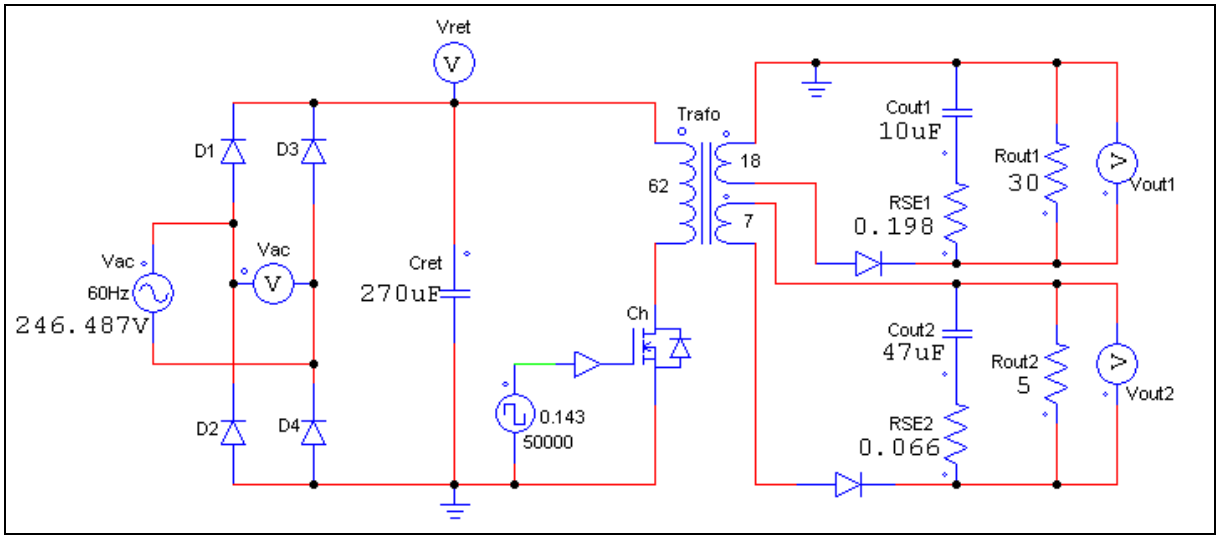


Figura 16 - Circuito para simulação com tensão média de entrada em Malha Aberta

A Figura 17 abaixo mostra as formas de onda da tensão de entrada e da tensão na saída do retificador em Malha Aberta.

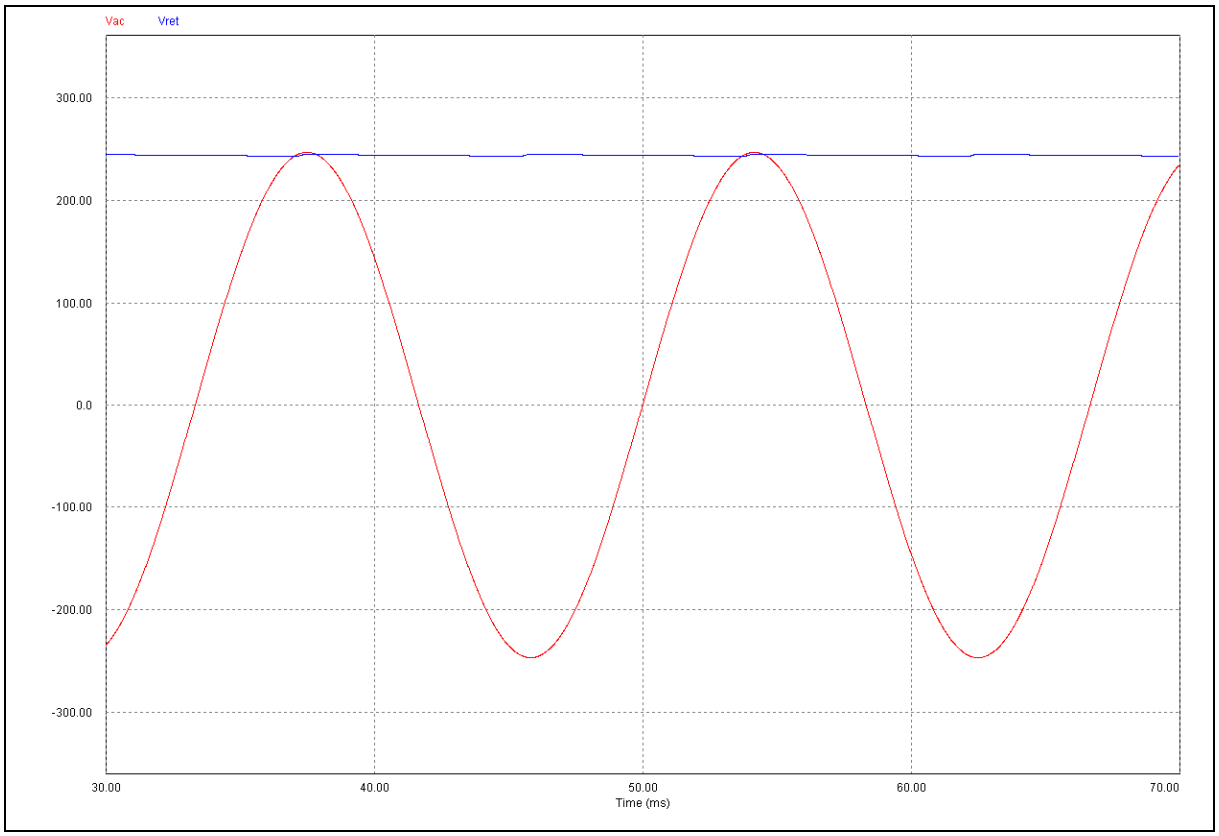


Figura 17 - Formas de onda da tensão de entrada e da tensão na saída do retificador com tensão média de entrada em Malha Aberta

A Figura 18 abaixo mostra o *ripple* da forma de onda da tensão na saída do retificador em Malha Aberta.

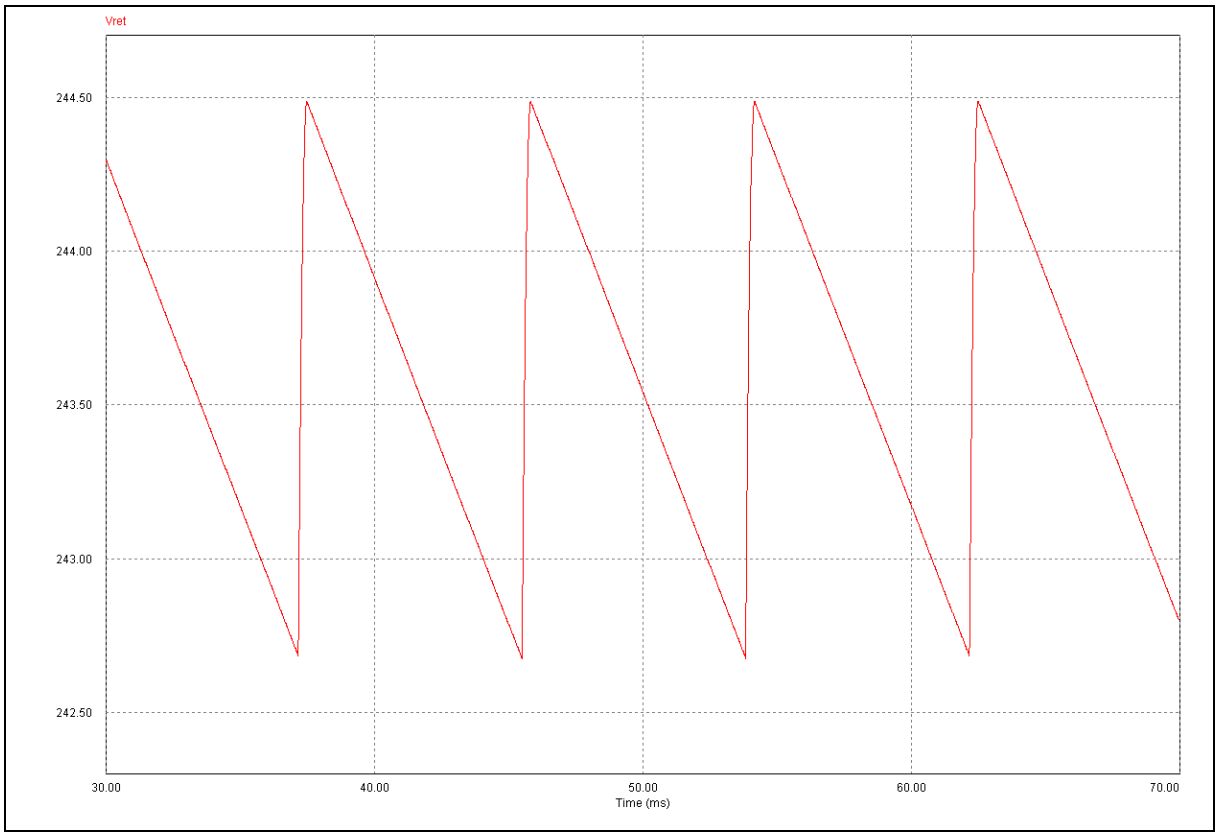


Figura 18 - *Ripple* da forma de onda da tensão na saída do retificador com tensão média de entrada em Malha Aberta

Vret máx = 244,487V

Vret min = 242,676V

Vret méd = 243,587V

A Figura 19 abaixo mostra, de forma ampliada, as formas de onda das correntes em dois diodos retificadores e da corrente na chave, com o circuito em Malha Aberta.

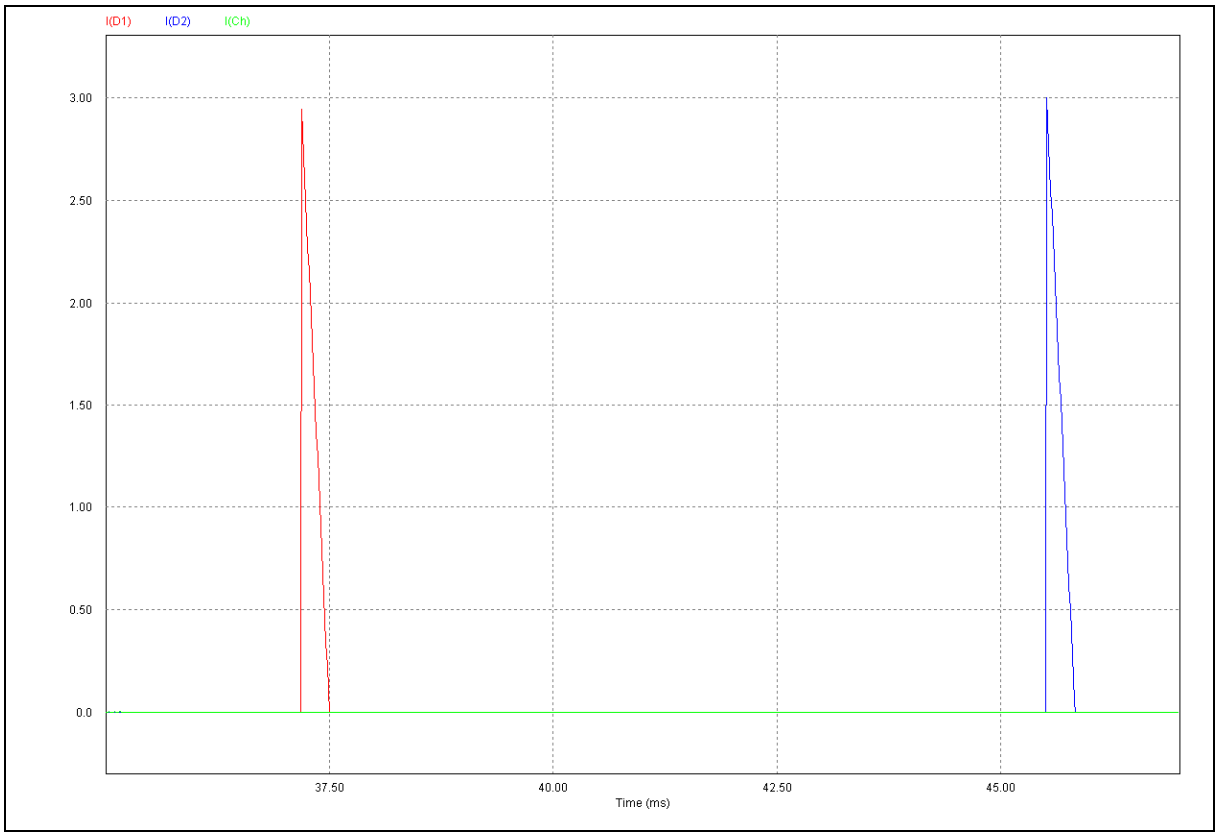


Figura 19 - Ampliação das formas de onda das correntes em dois diodos retificadores e da corrente na chave, com tensão média de entrada em Malha Aberta

Id1 pk = 2,94348A

Id2 pk = 2,99883A

A Figura 20 abaixo mostra as formas de onda das tensões e correntes nas duas saídas, em Malha Aberta.

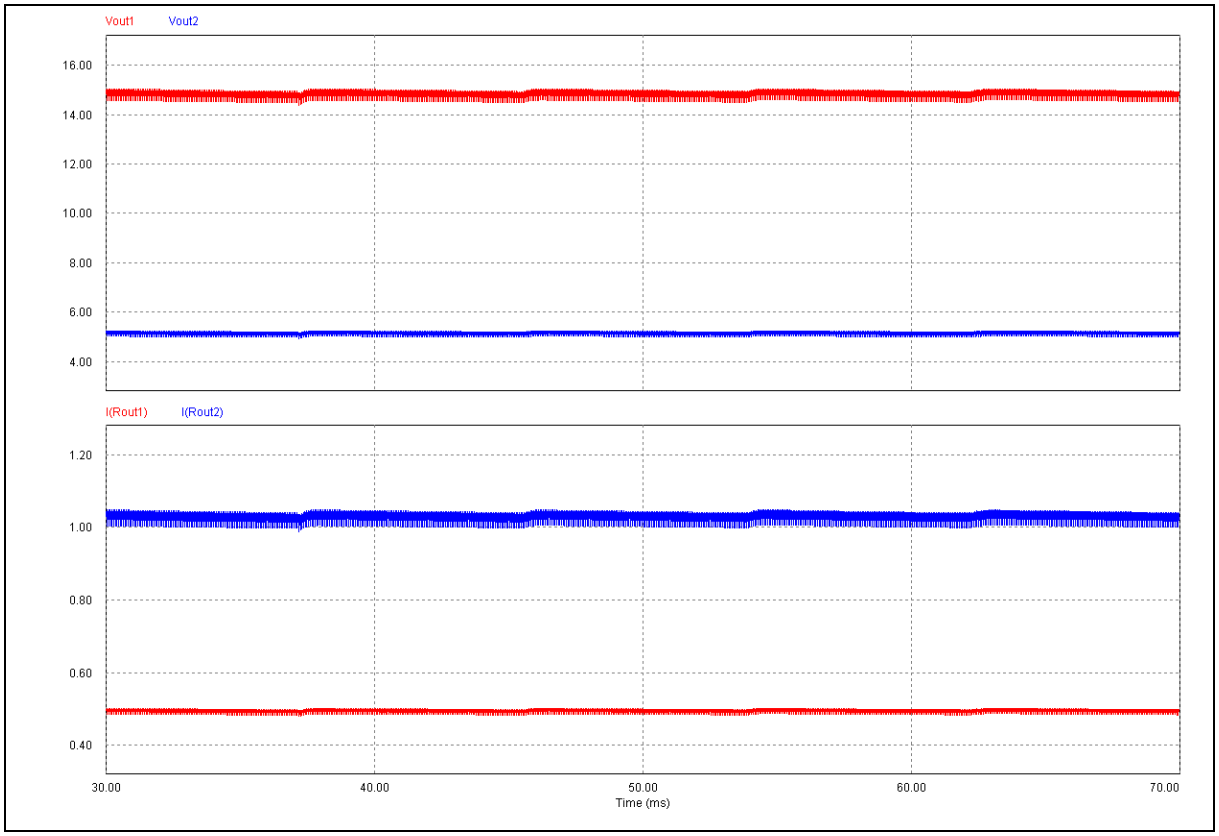


Figura 20 - Formas de onda das tensões e correntes nas duas saídas, com tensão média de entrada em Malha Aberta

Vout1 máx = 15,0498V

Vout1 min = 14,3712V

Vout1 méd = 14,8117V

Vout2 máx = 5,24085V

Vout2 min = 4,93967V

Vout2 méd = 5,13767V

Iout1 máx = 0,501661A

Iout1 min = 0,479041A

Iout1 méd = 0,493723A

Iout2 máx = 1,04817A

Iout2 min = 0,987935A

Iout2 méd = 1,02753ª

2.12.2 Simulação em Malha Fechada

Pelo fato da simulação com o circuito em Malha Fechada não ter sido satisfatória, foi simulado apenas para tensão média de entrada, para simular condições reais, e não extremas, da fonte.

A Figura 5, apresentada anteriormente, mostra o circuito utilizado para a simulação em Malha Fechada.

A Figura 21 abaixo mostra as formas de onda da tensão de entrada e da tensão na saída do retificador em Malha Fechada.

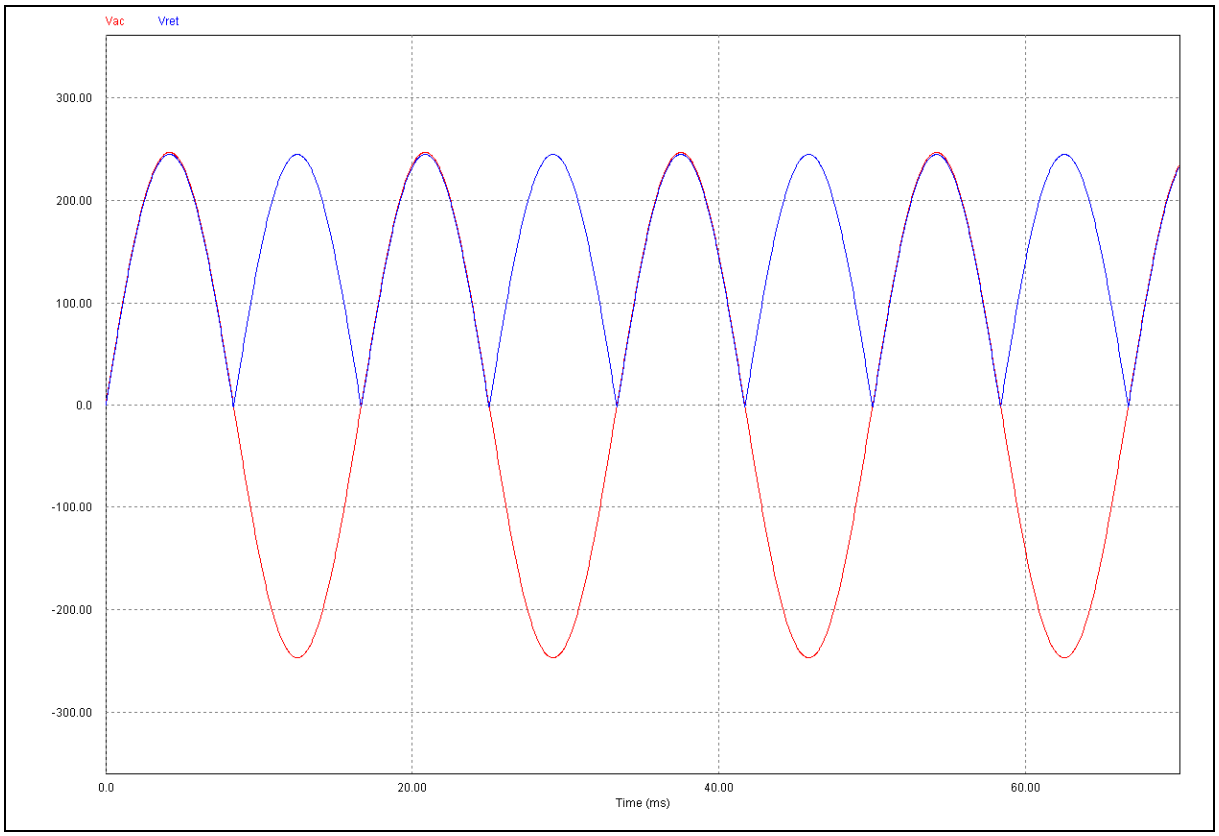


Figura 21 - Formas de onda da tensão de entrada e da tensão na saída do retificador em Malha Fechada

A Figura 22 abaixo mostra as formas de onda das correntes em dois diodos retificadores e da corrente na chave, com o circuito em Malha Fechada.

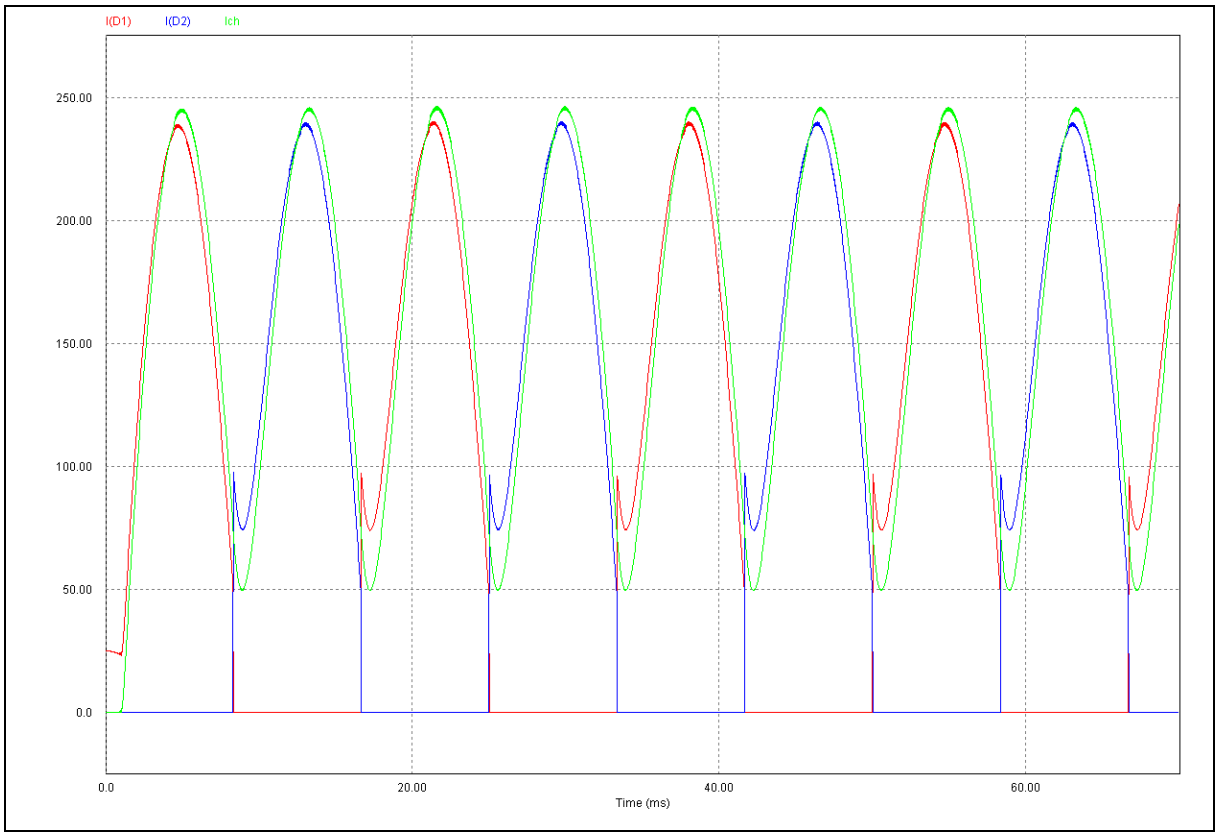


Figura 22 - Formas de onda das correntes em dois diodos retificadores e da corrente na chave, em Malha Fechada

A Figura 23 abaixo mostra as formas de onda das tensões e correntes nas duas saídas, em Malha Fechada.

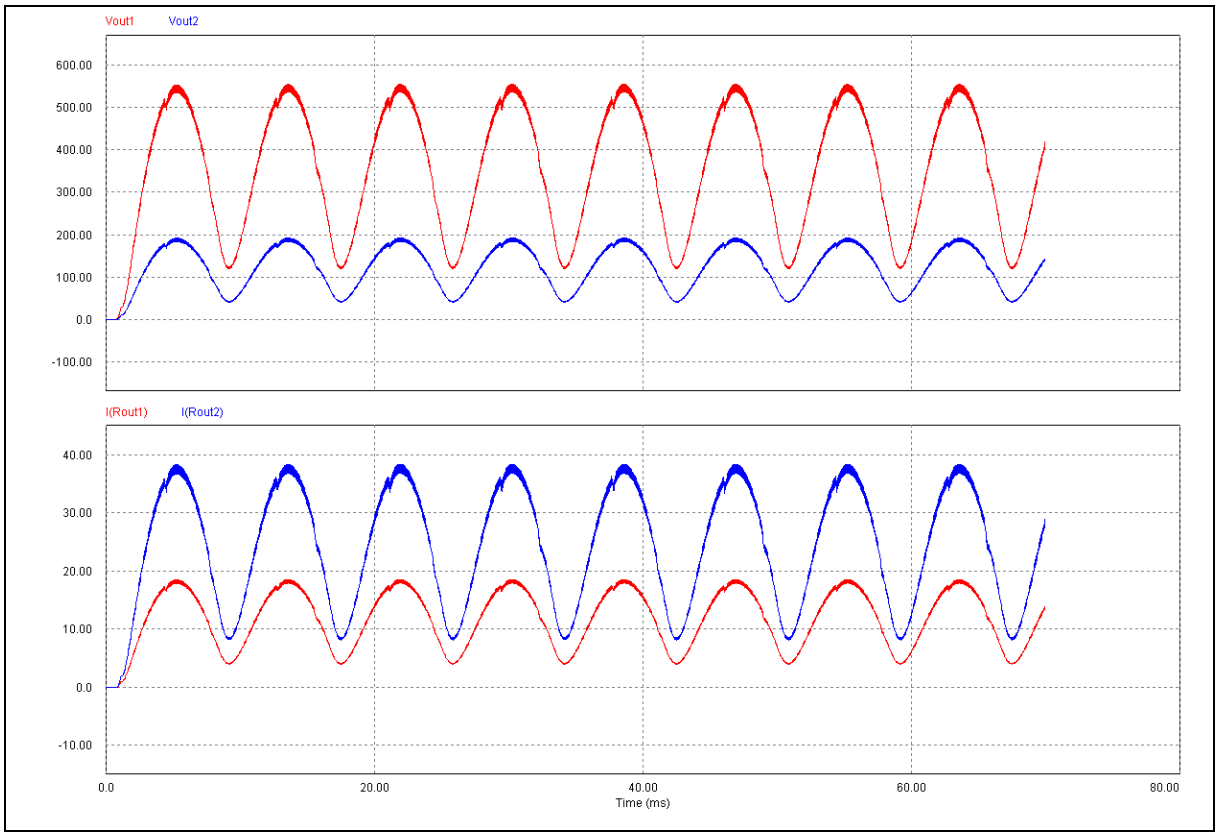


Figura 23 - Formas de onda das tensões e correntes nas duas saídas, em Malha Fechada

3. CONCLUSÕES

Neste relatório foi projetado um Conversor Flyback, com o circuito retificador de entrada com filtro capacitivo, o transformador, os componentes do estágio de potência, o comando e o controle do conversor. Bem como também foi realizada a simulação do circuito.

O projeto do retificador e do estágio de potência mostrou-se satisfatório, porém, para que este projeto possa ser implementado, serão necessários alguns ajustes, pois os valores de tensão e corrente obtidos na saída do conversor, encontrados na simulação, mostraram-se um pouco divergentes dos calculados, com valores apenas próximos dos requeridos e com oscilações não desprezíveis.

Quando foi aplicado o circuito de controle, os valores simulados mostraram-se totalmente divergentes da realidade. Infelizmente não foi possível encontrar soluções para que este problema fosse resolvido.

4. REFERÊNCIAS

BARBI, Ivo. *Eletrônica de Potência: Projeto de Fontes Chaveadas*. 1a. Edição. Florianópolis: Editora da UFSC, 2001. 332 p.

PETRY, Clóvis Antônio. *Projeto de um Conversor Flyback e de um Conversor Forward Isolados com Retificador e Filtro Capacitivo*. Publicação Interna. INEP/UFSC. Florianópolis, 2000.

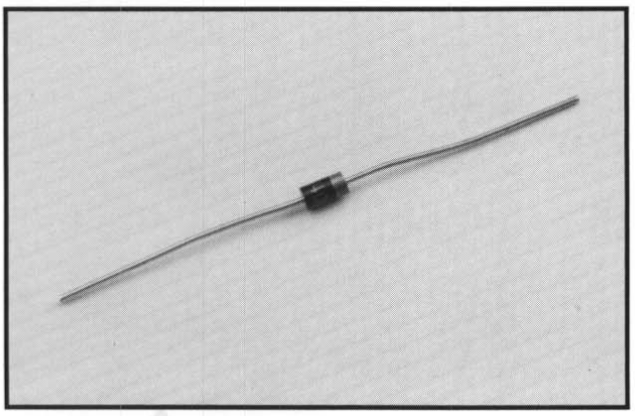
PETRY, Clóvis Antônio; PERAÇA, Mauro Tavares. *Apresentações das aulas do curso de Pós-Graduação em Desenvolvimento de Produtos Eletrônicos do IF-SC*. Florianópolis, 2009.

5. ANEXOS

5.1 *Datasheet* dos Diodos da ponte retificadora

1N4001 Thru 1N4007

1 AMP PLASTIC SILICON RECTIFIER

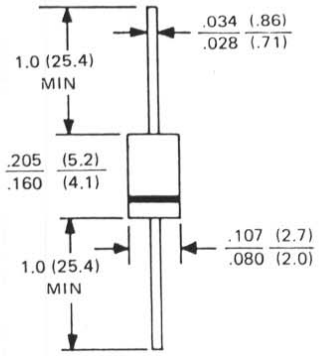


FEATURES

- Rating to 1000V PRV
- Low cost
- Diffused junction
- Low leakage
- Low forward voltage drop
- High current capability
- Easily cleaned with freon, alcohol, chlorothene and similar solvents
- UL recognized 94V-O plastic material

Outline Drawing

DO-41



Dimensions in inches and (millimeters)

Mechanical Data

- Case: JEDEC DO-41
- Terminals: Axial leads, solderable per MIL-STD-202, Method 208
- Polarity: Color band denotes cathode
- Weight: 0.012 ounce, 0.3 grams
- Mounting Position: Any

Maximum Ratings & Characteristics

- Ratings at 25° C ambient temperature unless otherwise specified
- Single phase, half wave, 60Hz, resistive or inductive load
- For capacitive load, derate current by 20%

		1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	Units
Maximum Recurrent Peak Reverse Voltage	V_{RRM}	50	100	200	400	600	800	1000	V
Maximum RMS Voltage	V_{RMS}	35	70	140	280	420	560	700	V
Maximum DC Blocking Voltage	V_{DC}	50	100	200	400	600	800	1000	V
Maximum Average Forward Rectified Current .375 (9.5mm) Lead Lengths @ T_A = 75° C	$I_{(AV)}$	1.0							A
Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave Superimposed On Rated Load	I_{FSM}	40							A
Maximum Forward Voltage At 1.0A DC	V_F	1.0							V
Maximum DC Reverse Current @ T_A = 25°C At Rated DC Blocking Voltage @ T_A = 100°C	I_R	5 50							μA
Typical Junction Capacitance (Note 1) T_A = 25° C	C_J	15							pF
Typical Thermal Resistance (Note 2)	R_{thJA}	26							°C/W
Operating Temperature Range	T_J	-65 to +175							°C
Storage Temperature Range	T_{STG}	-65 to +175							°C

Notes: 1. Measured at 1.0 MHz and applied reverse voltage of 4.0V DC

5.2 *Datasheet* do Interruptor

HARRIS SEMICONDUCTOR

IRF740, IRF741, IRF742, IRF743

8A and 10A, 350V and 400V, 0.55 and 0.80 Ohm, N-Channel Power MOSFETs

July 1998

Features

- 8A and 10A, 350V and 400V
- $r_{DS(ON)}$ = 0.55Ω and 0.80Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Description

These are N-Channel enhancement mode silicon gate power field effect transistors. These types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. They can be operated directly from integrated circuits.

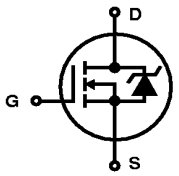
Formerly developmental type TA17424.

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRF740D	TO-220AB	IRF740
IRF741	TO-220AB	IRF741
IRF742	TO-220AB	IRF742
IRF743	TO-220AB	IRF743

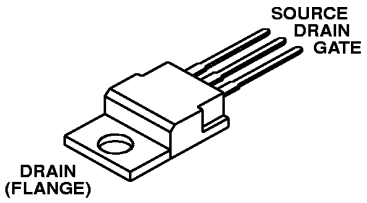
NOTE: When ordering, include the entire part number.

Symbol



Packaging

JEDEC TO-220AB
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

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File Number **2311.2**

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Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		IRF740	IRF741	IRF742	IRF743	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	400	350	400	350	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	400	350	400	350	V
Continuous Drain Current	ID	10	10	8.0	8.0	A
$T_C = 100^oC$	I_D	6.3	6.3	5.2	5.2	A
Pulsed Drain Current (Note 3)	I_{DM}	40	40	33	33	A
Gate to Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation	P_D	125	125	125	125	W
Linear Derating Factor		1.0	1.0	1.0	1.0	$W/^oC$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	520	520	520	520	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering						
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	300	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	260	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA (Figure 10)				
IRF740, IRF742			400	-	-	V
IRF741, IRF743			350	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$	-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V				
IRF740, IRF741			10	-	-	A
IRF742, IRF743			8.3	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±500	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.2A (Figures 8, 9)				
IRF740, IRF741			-	0.47	0.55	Ω
IRF742, IRF743			-	0.68	0.80	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V$, I_D = 5.2A (Figure 12)	5.8	8.9	-	S
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 200V, $I_D \approx$ 10A, R_G = 9.1Ω, R_L = 20Ω, V_{GS} = 10V, (Figures 17, 18) MOSFET switching times are essentially independent of operating temperature	-	15	21	ns
Rise Time	t_r		-	25	41	ns
Turn-Off Delay Time	$t_{D(OFF)}$		-	52	75	ns
Fall Time	t_f		-	25	36	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 x Rated BV_{DSS} $I_{g(REF)}$ = 1.5mA (Figures 14, 19, 20) Gate charge is essentially independent of operating temperature	-	41	63	nC
Gate to Source Charge	Q_{gs}		-	6.5	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	23	-	nC

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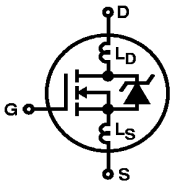
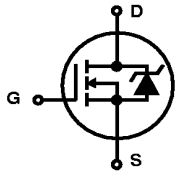
Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz (Figure 11)		-	1250	-	pF
Output Capacitance	C_{OSS}			-	300	-	pF
Reverse-Transfer Capacitance	C_{RSS}			-	80	-	pF
Internal Drain Inductance	L_D	Measured From the Contact Screw on Tab to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	3.5	-	nH
		Measured From The Drain Lead, 6mm (0.25in) From Package to Center of Die		-	4.5	-	nH
Internal Source Inductance	L_S	Measured From The Source Lead, 6mm (0.25in) From Header to Source Bonding Pad		-	7.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta CS}$			-	-	1.0	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	62.5	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	10	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	40	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, I_{SD} = 10A, V_{GS} = 0V (Figure 13)		-	-	2.0	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, I_{SD} = 10A, dI_{SD}/dt = 100A/μs		170	390	790	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 25^oC$, I_{SD} = 10A, dI_{SD}/dt = 100A/μs		1.6	4.5	8.2	μC

NOTES:

2. Pulse Test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. V_{DD} = 50V, starting $T_J = 25^oC$, L = 9.1μH, R_G = 25Ω, peak I_{AS} = 10A. See Figures 15 and 16.

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Typical Performance Curves Unless Otherwise Specified

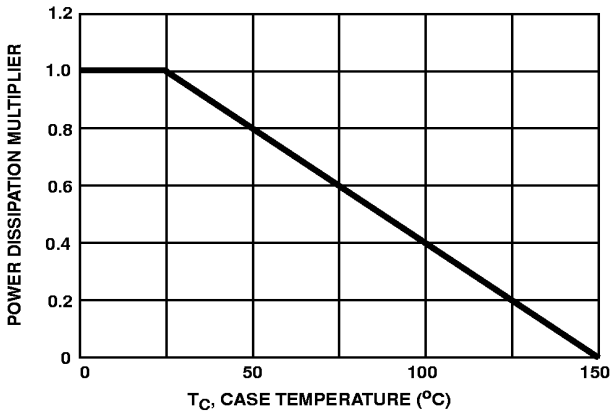

FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

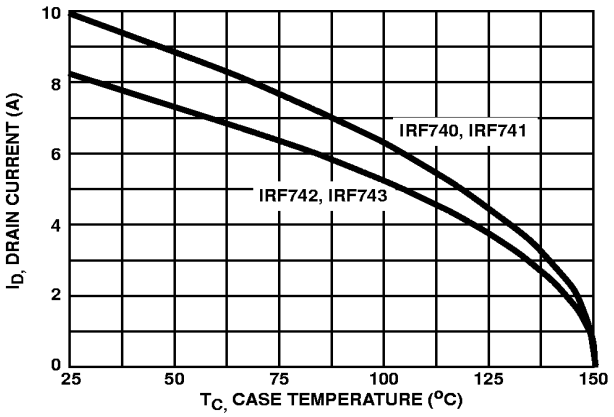

FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

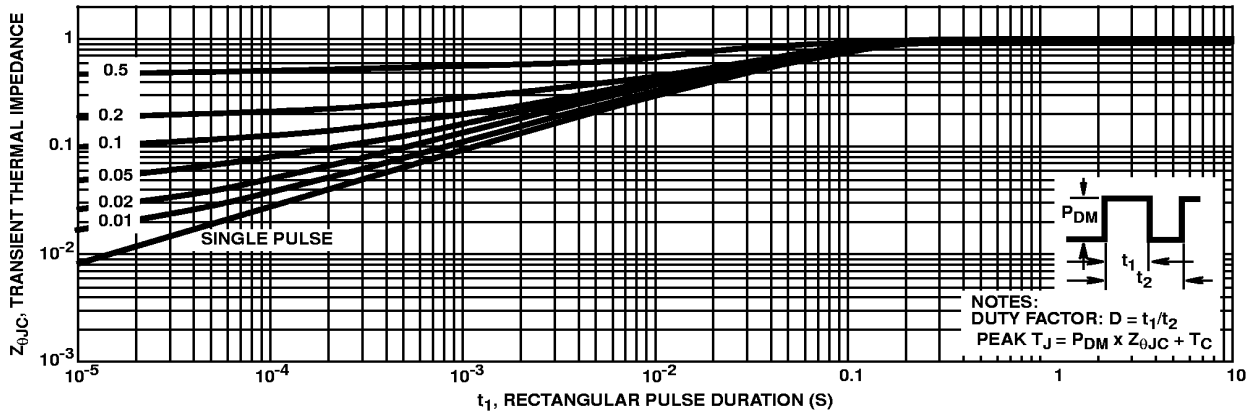

FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

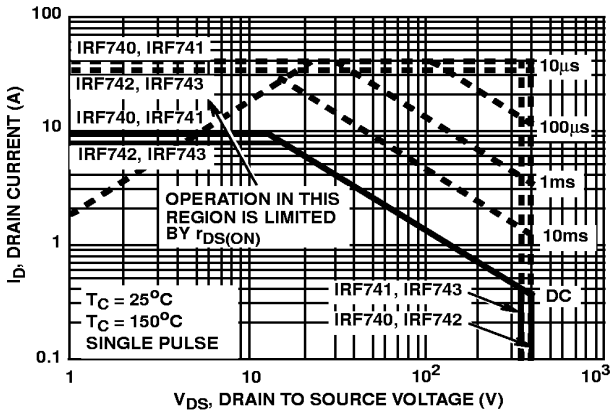

FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

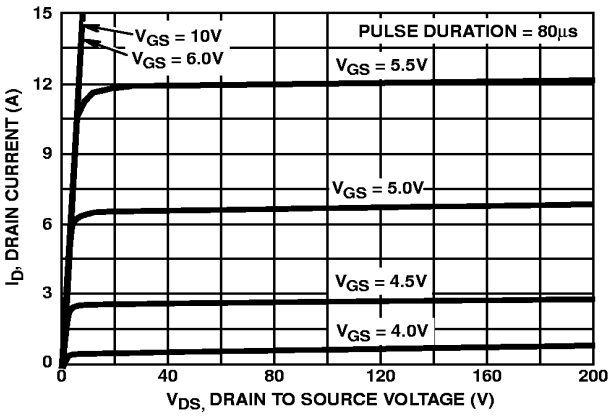

FIGURE 5. OUTPUT CHARACTERISTICS

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Typical Performance Curves Unless Otherwise Specified (Continued)

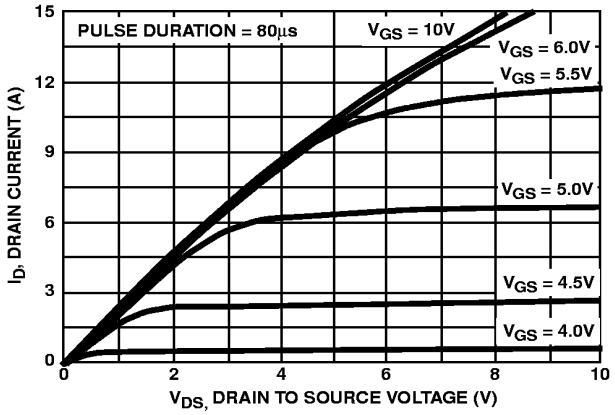

FIGURE 6. SATURATION CHARACTERISTICS

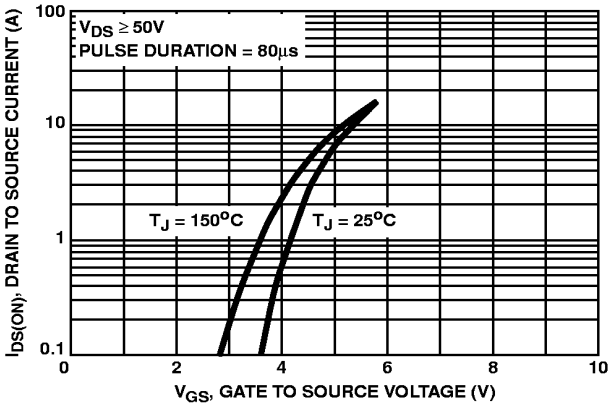

FIGURE 7. TRANSFER CHARACTERISTICS

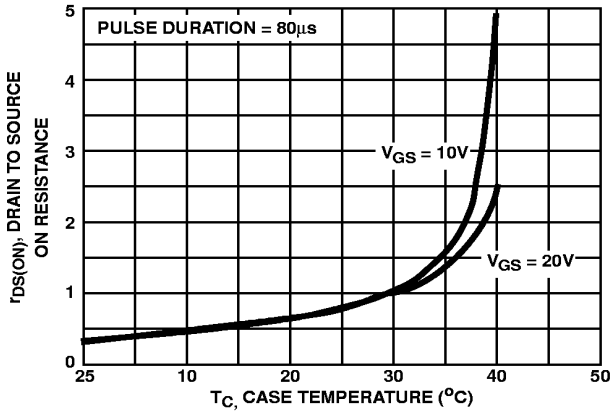

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

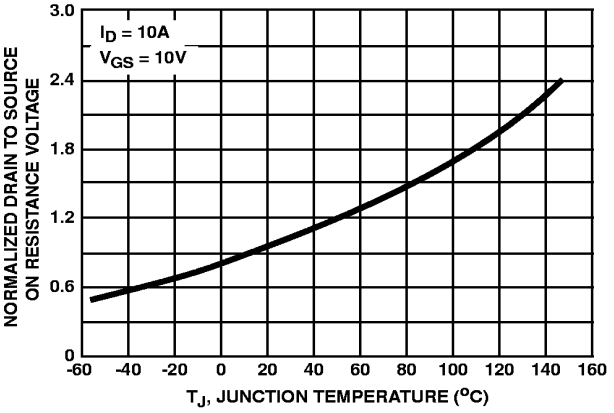

FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

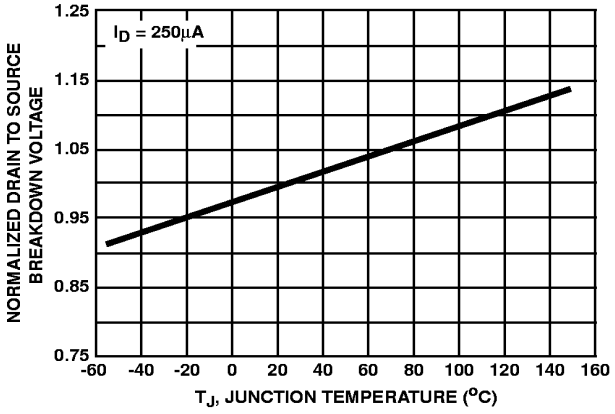

FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

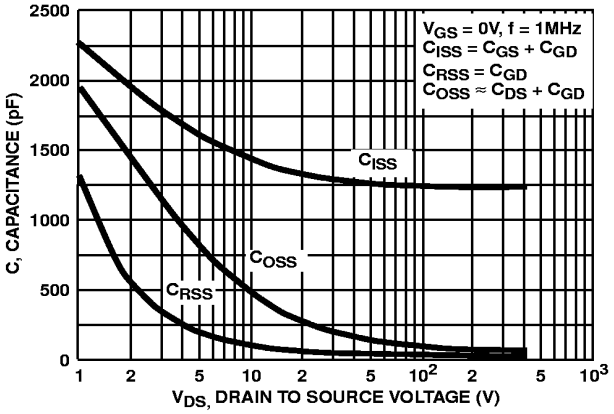

FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

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Typical Performance Curves Unless Otherwise Specified (Continued)

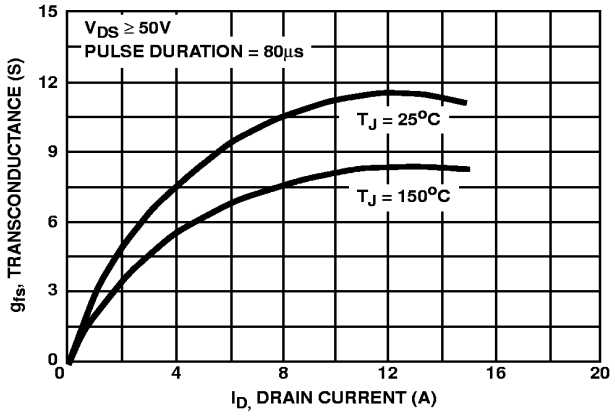

FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

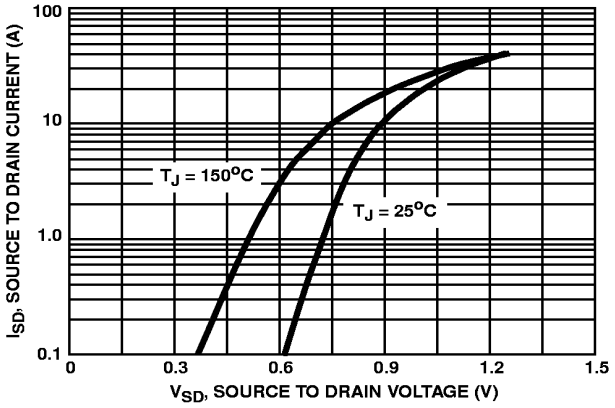

FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

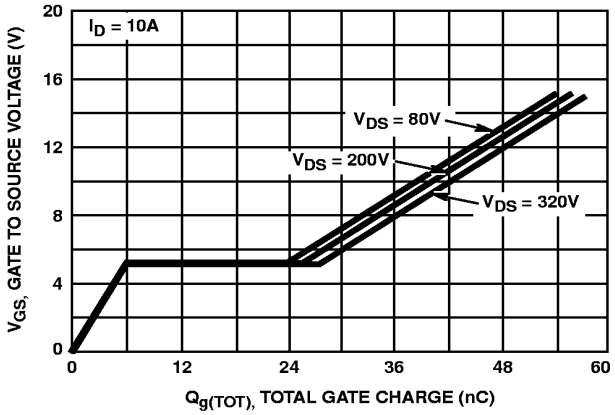

FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

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Test Circuits and Waveforms

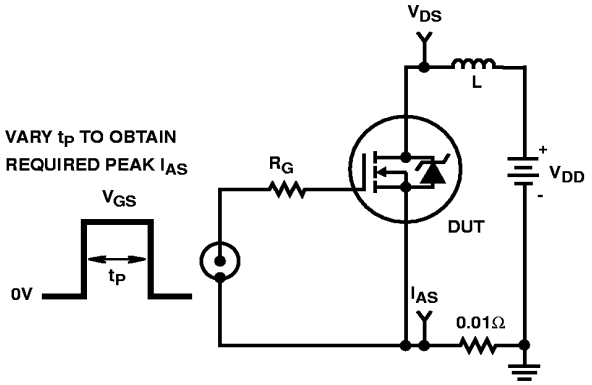

FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

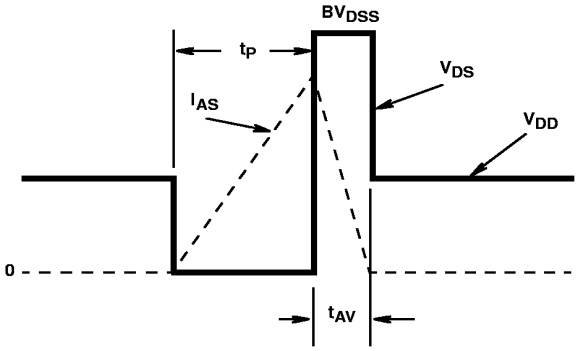

FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

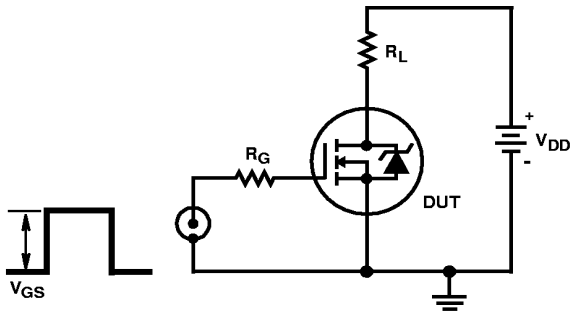

FIGURE 17. SWITCHING TIME TEST CIRCUIT

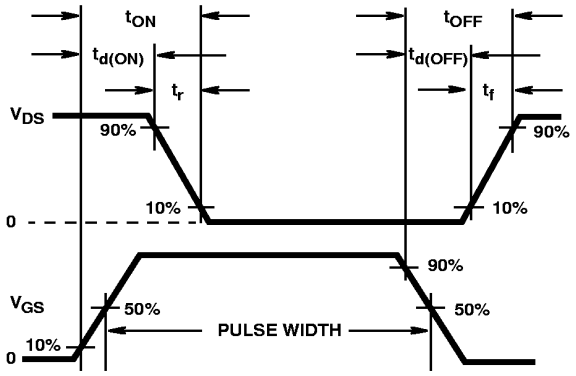

FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

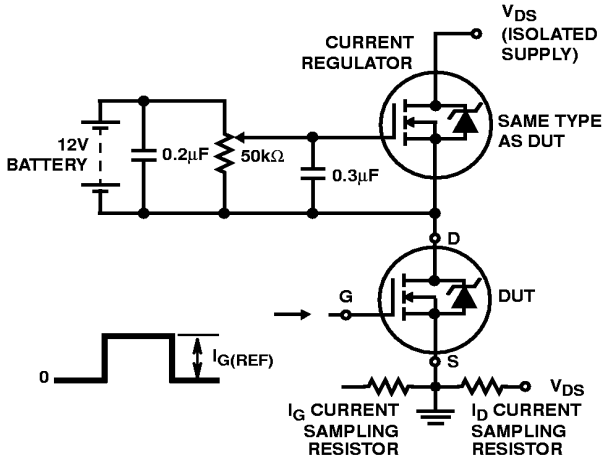

FIGURE 19. GATE CHARGE TEST CIRCUIT

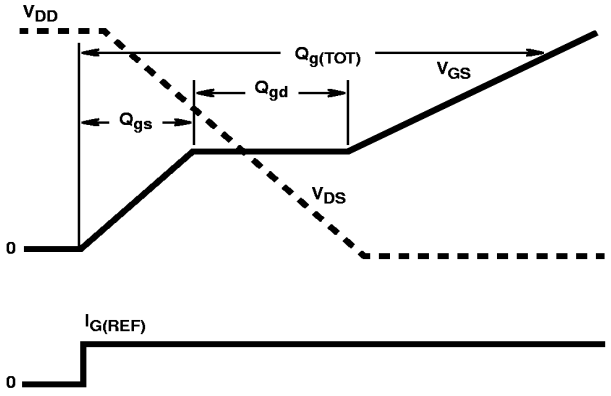

FIGURE 20. GATE CHARGE WAVEFORMS

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5.3 *Datasheet* dos Diodos MUR810 e MUR805

MUR805, MUR810, MUR815, MUR820, MUR840, MUR860

Preferred Devices

SWITCHMODE™ Power Rectifiers

. . . designed for use in switching power supplies, inverters and as free wheeling diodes, these state–of–the–art devices have the following features:

- Ultrafast 25, 50 and 75 Nanosecond Recovery Time
- 175°C Operating Junction Temperature
- Popular TO–220 Package
- Epoxy Meets UL94, V_O @ 1/8″
- Low Forward Voltage
- Low Leakage Current
- High Temperature Glass Passivated Junction
- Reverse Voltage to 600 Volts

Mechanical Characteristics:

- Case: Epoxy, Molded
- Weight: 1.9 grams (approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead Temperature for Soldering Purposes: 260°C Max. for 10 Seconds
- Shipped 50 units per plastic tube
- Marking: U805, U810, U815, U820, U840, U860

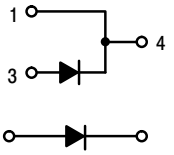
MAXIMUM RATINGS

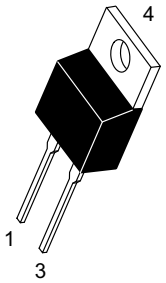
Please See the Table on the Following Page

ON Semiconductor™

http://onsemi.com

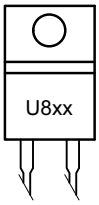
ULTRAFAST RECTIFIERS 8.0 AMPERES 50–600 VOLTS





CASE 221B
TO–220AC
PLASTIC

MARKING DIAGRAM



U8xx = Device Code
xx = 05, 10, 15, 20, 40 or 60

ORDERING INFORMATION

Device	Package	Shipping
MUR805	TO–220	50 Units/Rail
MUR810	TO–220	50 Units/Rail
MUR815	TO–220	50 Units/Rail
MUR820	TO–220	50 Units/Rail
MUR840	TO–220	50 Units/Rail
MUR860	TO–220	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

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MAXIMUM RATINGS

Rating	Symbol	MUR 805	MUR 810	MUR 815	MUR 820	MUR 840	MUR 860	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	150	200	400	600	Volts
Average Rectified Forward Current Total Device, (Rated V_R), T_C = 150°C	$I_{F(AV)}$	8.0						Amps
Peak Repetitive Forward Current (Rated V_R, Square Wave, 20 kHz), T_C = 150°C	I_{FM}	16						Amps
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions halfwave, single phase, 60 Hz)	I_{FSM}	100						Amps
Operating Junction Temperature and Storage Temperature Range	T_J, T_{stg}	–65 to +175						°C

THERMAL CHARACTERISTICS

Maximum Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.0	2.0	°C/W

ELECTRICAL CHARACTERISTICS

Maximum Instantaneous Forward Voltage (Note 1.) (i_F = 8.0 Amps, T_C = 150°C) (i_F = 8.0 Amps, T_C = 25°C)	v_F	0.895 0.975	1.00 1.30	1.20 1.50	Volts
Maximum Instantaneous Reverse Current (Note 1.) (Rated dc Voltage, T_J = 150°C) (Rated dc Voltage, T_J = 25°C)	i_R	250 5.0	500 10		μA
Maximum Reverse Recovery Time (I_F = 1.0 Amp, di/dt = 50 Amps/μs) (I_F = 0.5 Amp, i_R = 1.0 Amp, I_{REC} = 0.25 Amp)	t_{rr}	35 25	60 50		ns

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

MUR805, MUR810, MUR815, MUR820

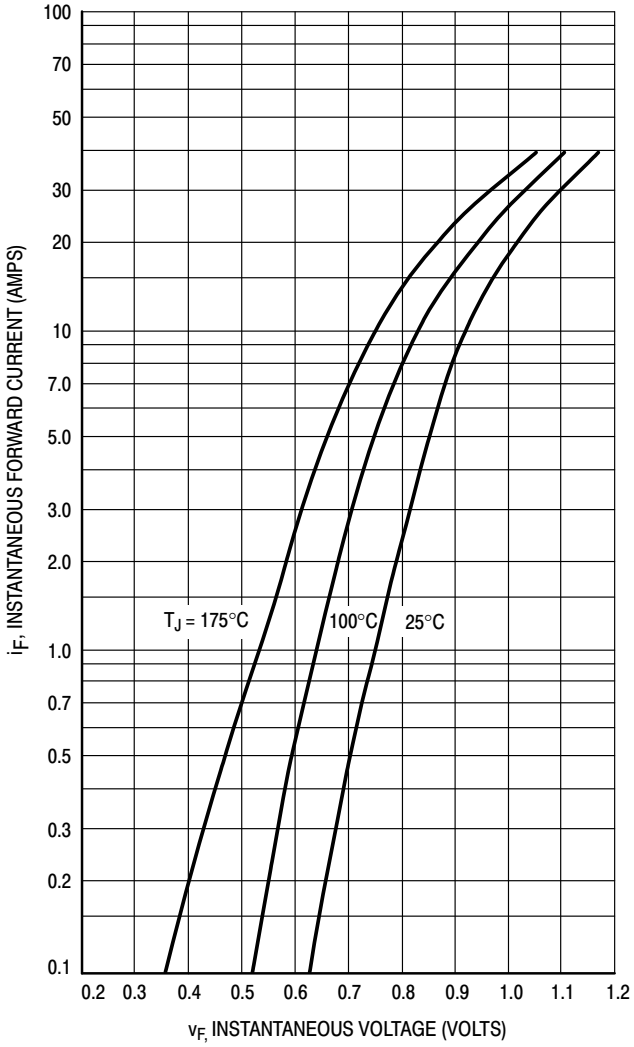


Figure 1. Typical Forward Voltage

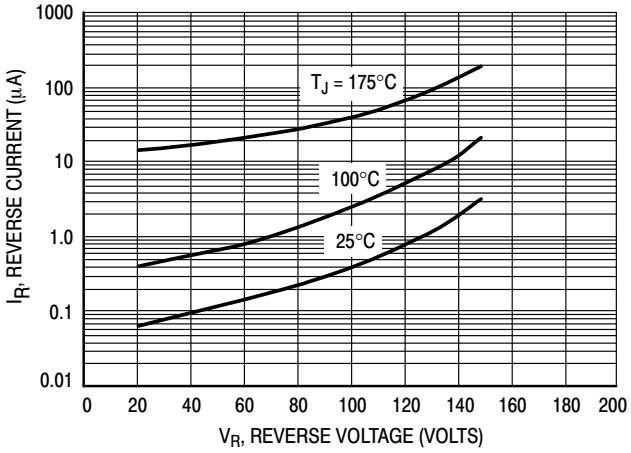


Figure 2. Typical Reverse Current*

* The curves shown are typical for the highest voltage device in the grouping. Typical reverse current for lower voltage selections can be estimated from these same curves if V_R is sufficiently below rated V_R.

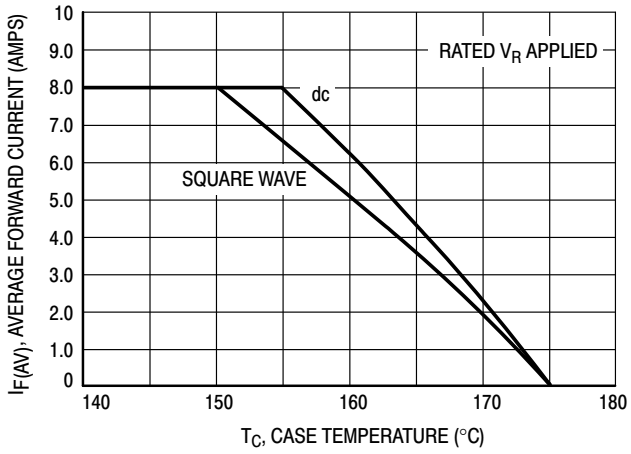


Figure 3. Current Derating, Case

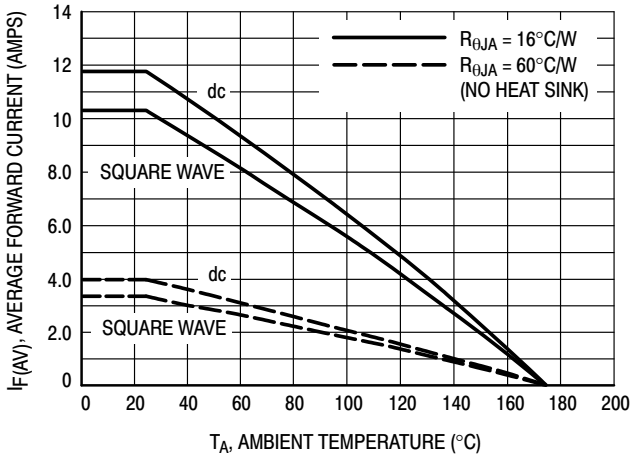


Figure 4. Current Derating, Ambient

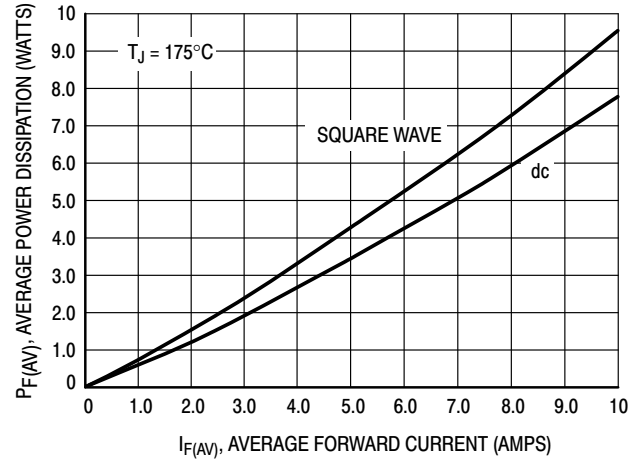


Figure 5. Power Dissipation

MUR840

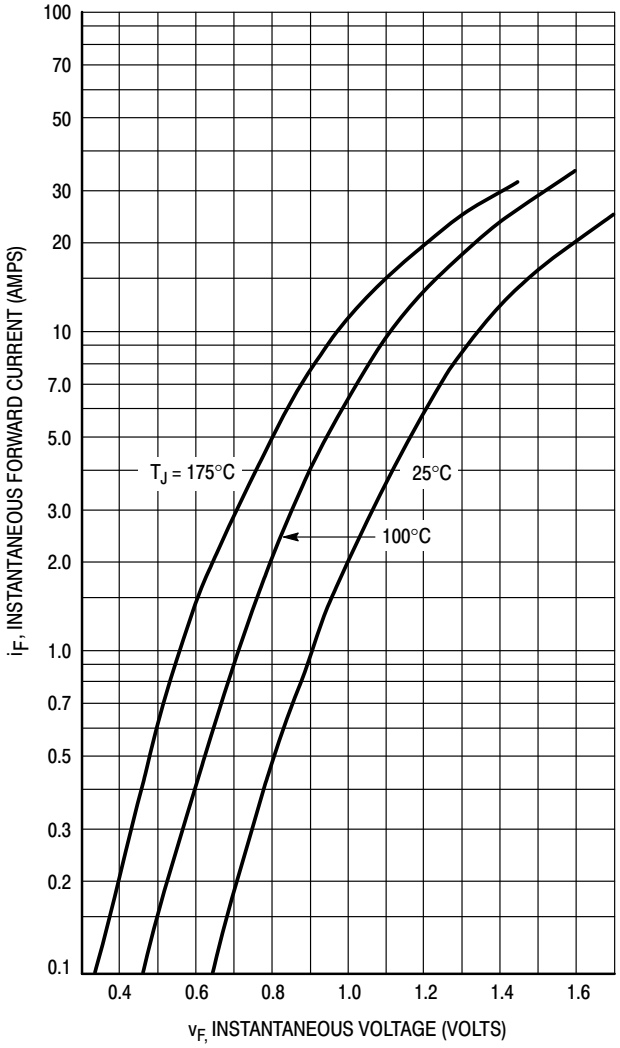


Figure 6. Typical Forward Voltage

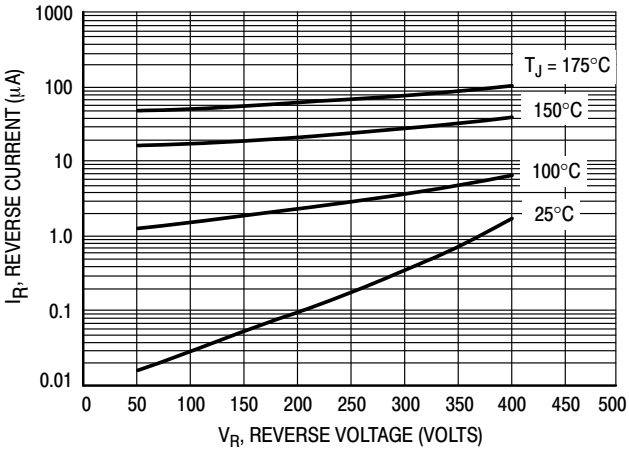


Figure 7. Typical Reverse Current*

* The curves shown are typical for the highest voltage device in the grouping. Typical reverse current for lower voltage selections can be estimated from these same curves if V_R is sufficiently below rated V_R.

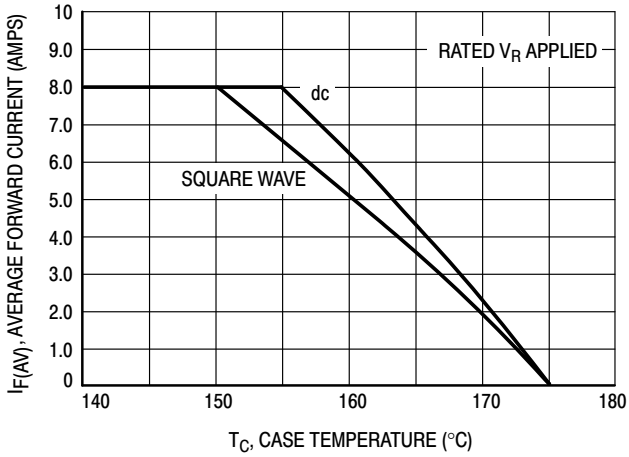


Figure 8. Current Derating, Case

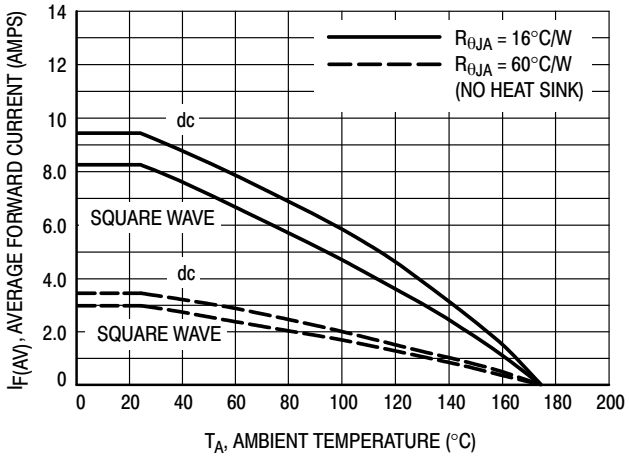


Figure 9. Current Derating, Ambient

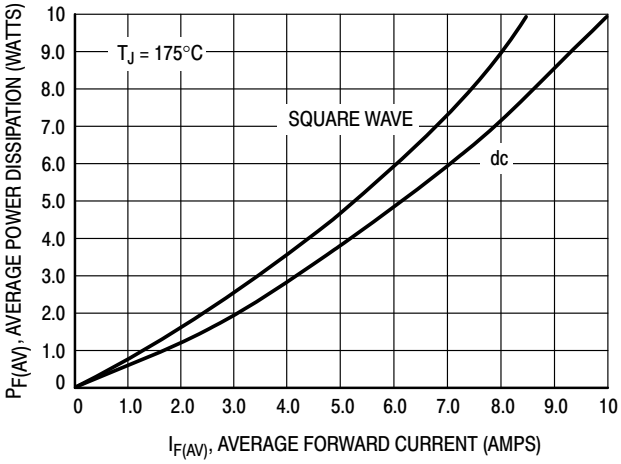


Figure 10. Power Dissipation

MUR860

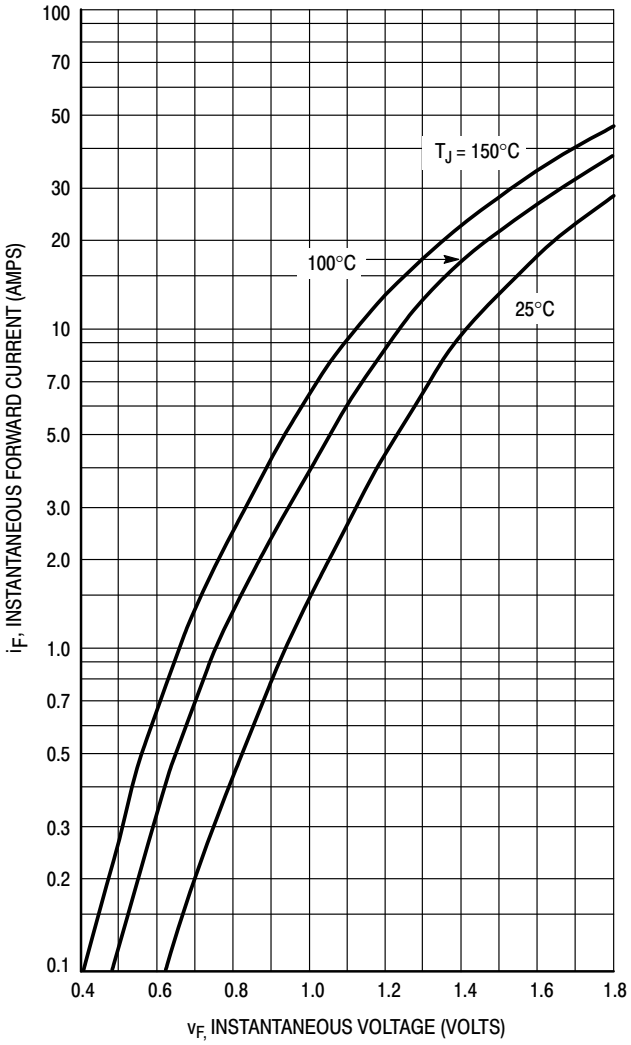


Figure 11. Typical Forward Voltage

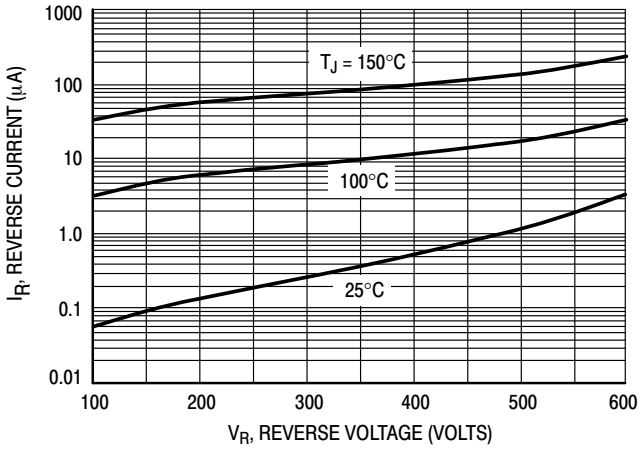


Figure 12. Typical Reverse Current*

* The curves shown are typical for the highest voltage device in the grouping. Typical reverse current for lower voltage selections can be estimated from these same curves if V_R is sufficiently below rated V_R.

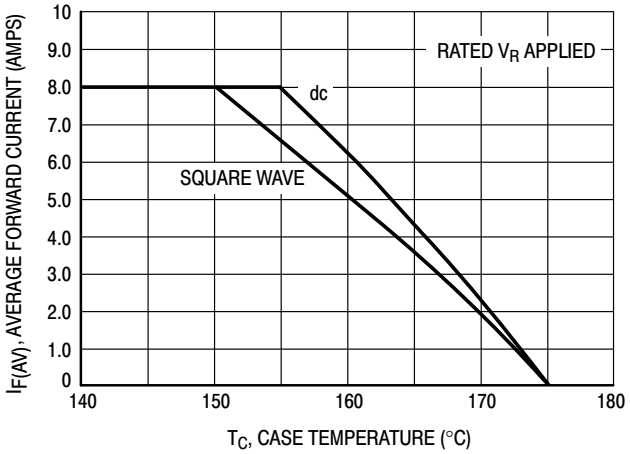


Figure 13. Current Derating, Case

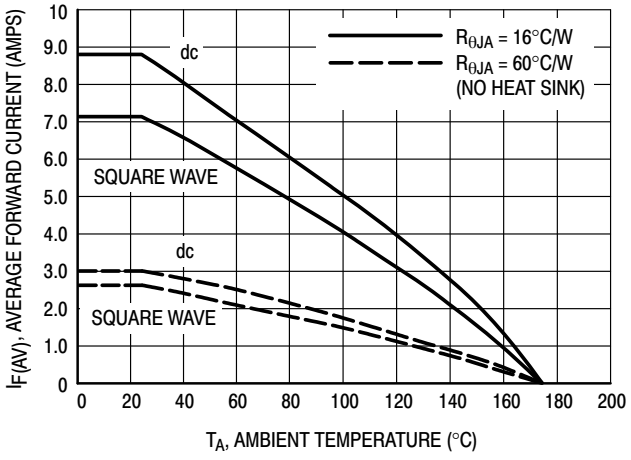


Figure 14. Current Derating, Ambient

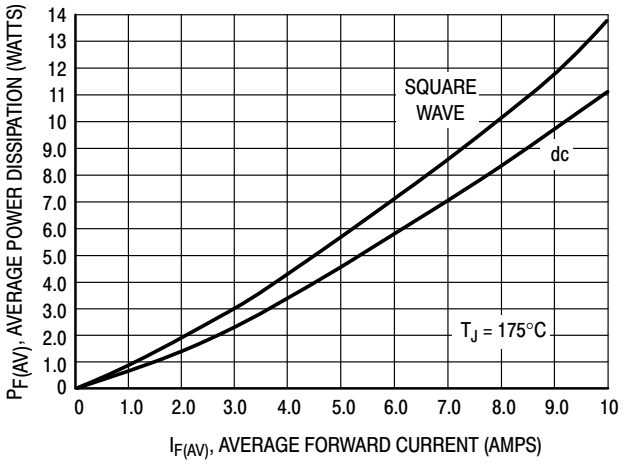


Figure 15. Power Dissipation

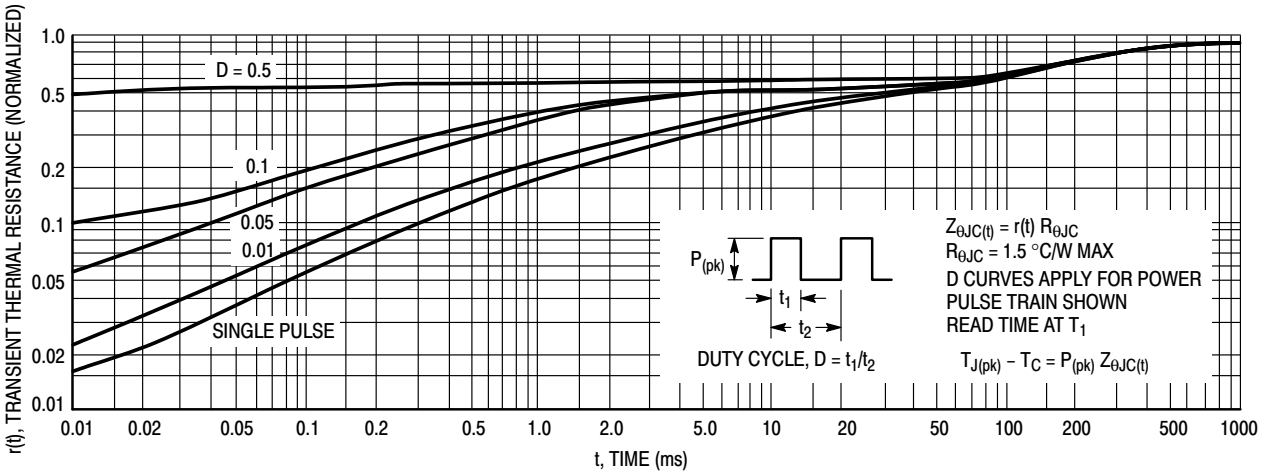


Figure 16. Thermal Response

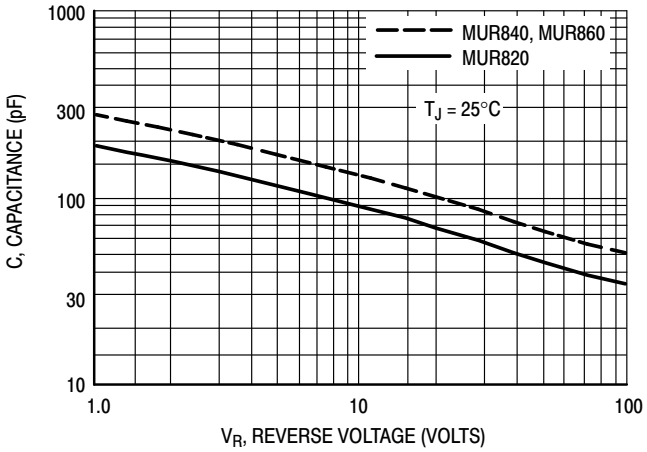
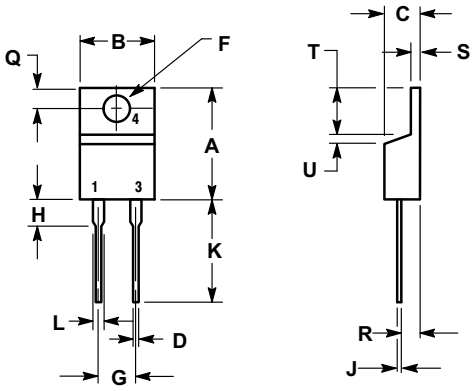


Figure 17. Typical Capacitance

PACKAGE DIMENSIONS

TO–220 TWO–LEAD
CASE 221B–04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.595	0.620	15.11	15.75
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.82
D	0.025	0.035	0.64	0.89
F	0.142	0.147	3.61	3.73
G	0.190	0.210	4.83	5.33
H	0.110	0.130	2.79	3.30
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.14	1.39
T	0.235	0.255	5.97	6.48
U	0.000	0.050	0.000	1.27

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5.4 *Datasheet* do Circuito Integrado UC 3524

Unitrode Products
from Texas Instruments

UC1524
UC2524
UC3524

Advanced Regulating Pulse Width Modulators

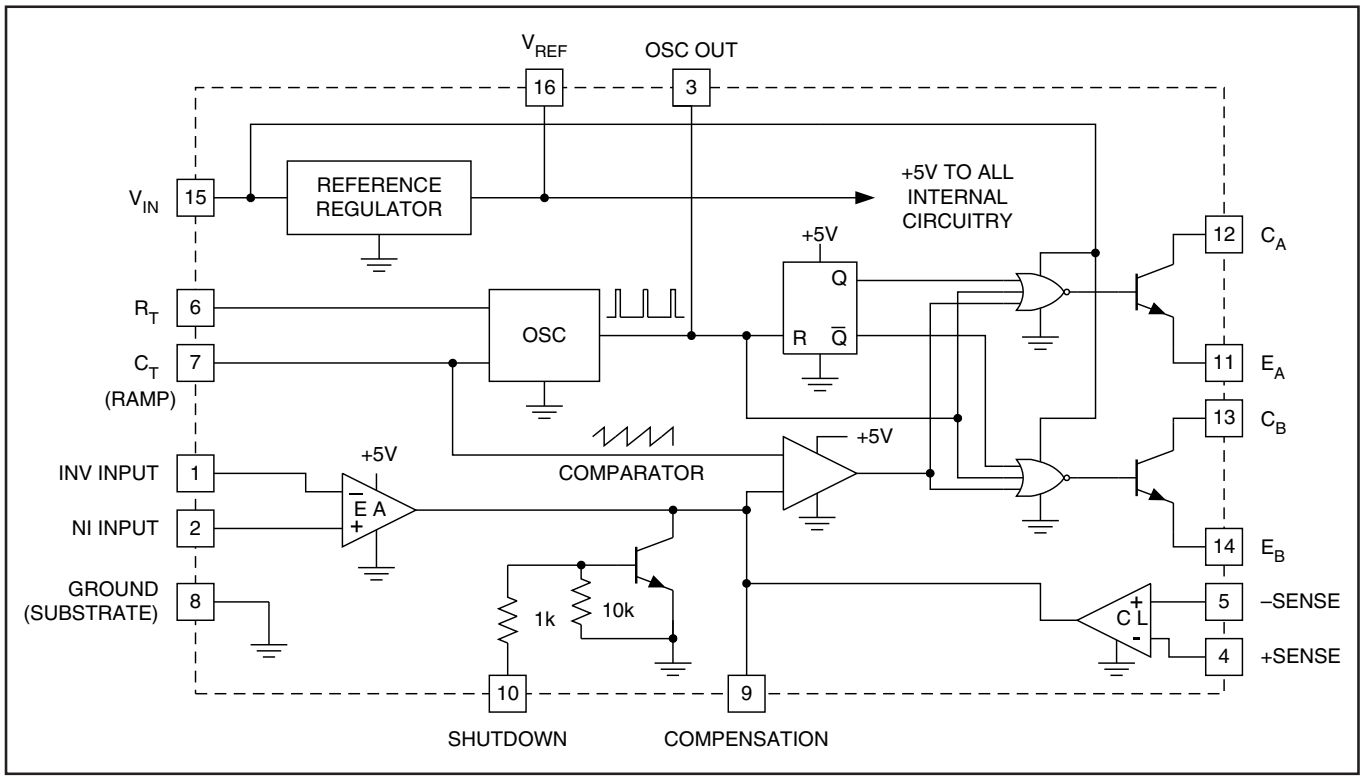
FEATURES

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-ended or Push-pull Applications
- Low Standby Current…8mA Typical
- Interchangeable with SG1524, SG2524 and SG3524, Respectively

DESCRIPTION

The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies, inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2524 and UC3524 are designed for operation from -25°C to +85°C and 0° to +70°C, respectively.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

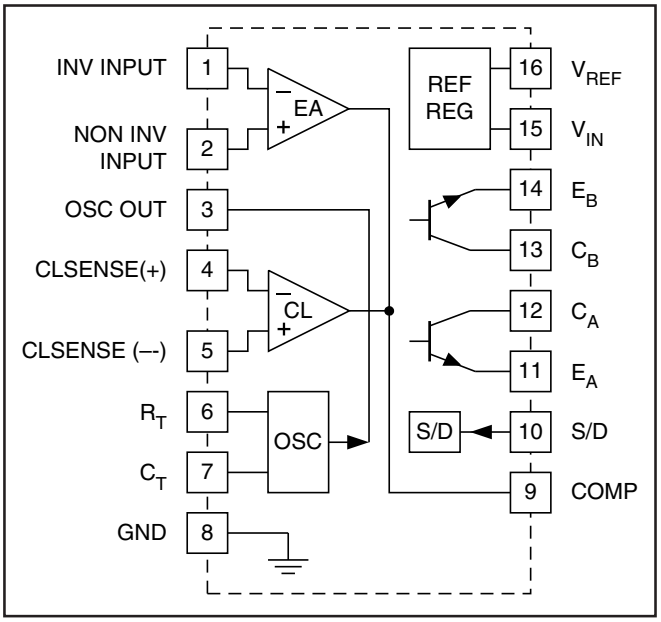
Supply Voltage, V_{CC} (Notes 2 and 3) 40V
Collector Output Current. 100mA
Reference Output Current 50mA
Current Through C_T Terminal . . . . . –5mA
Power Dissipation at T_A = +25°C (Note 4). 1000mW
Power Dissipation at T_C = +25°C (Note 4). 2000mW
Operating Junction Temperature Range . . . . –55°C to +150°C
Storage Temperature Range . . . . . –65°C to +150°C

Note 1: Over operating free-air temperature range unless otherwise noted.
Note 2: All voltage values are with respect to the ground terminal, pin 8.
Note 3: The reference regulator may be bypassed for operation from a fixed 5V supply by connecting the V_{CC} and reference output pins both to the supply voltage. In this configuration the maximum supply voltage is 6V.
Note 4: Consult packaging section of databook for thermal limitations and considerations of package.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC}. . . . . 8V to 40V
Reference Output Current . . . . . 0 to 20mA
Current through C_T Terminal . . . . . –0.03mA to –2mA
Timing Resistor, R_T . . . . . 1.8kΩ to 100kΩ
Timing Capacitor, C_T . . . . . 0.001µF to 0.1µF
Operating Ambient Temperature Range
UC1524 . . . . . –55°C to +125°C
UC2524 . . . . . –25°C to +85°C
UC3524 . . . . . 0°C to +70°C

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1524, –25°C to +85°C for the UC2524, and 0°C to +70°C for the UC3524, V_{IN} = 20V, and f = 20kHz, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNITS
		MIN		MAX	MIN		MAX	
Reference Section								
Output Voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	V_{IN} = 8 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Ripple Rejection	f = 120Hz, T_J = 25°C		66			66		dB
Short Circuit Current Limit	V_{REF} = 0, T_J = 25°C		100			100		mA
Temperature Stability	Over Operating Temperature Range		0.3	1		0.3	1	%
Long Term Stability	T_J = 125°C, t = 1000 Hrs.		20			20		mV
Oscillator Section								
Maximum Frequency	C_T = .001mfd, R_T = 2kΩ		300			300		kHz
Initial Accuracy	R_T and C_T Constant		5			5		%
Voltage Stability	V_{IN} = 8 to 40V, T_J = 25°C			1			1	%
Temperature Stability	Over Operating Temperature Range			5			5	%
Output Amplitude	Pin 3, T_J = 25°C		3.5			3.5		V
Output Pulse Width	C_T = .01mfd, T_J = 25°C		0.5			0.5		µs
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 2.5V		0.5	5		2	10	mV
Input Bias Current	V_{CM} = 2.5V		2	10		2	10	µA
Open Loop Voltage Gain		72	80		60	80		dB
Common Mode Voltage	T_J = 25°C	1.8		3.4	1.8		3.4	V

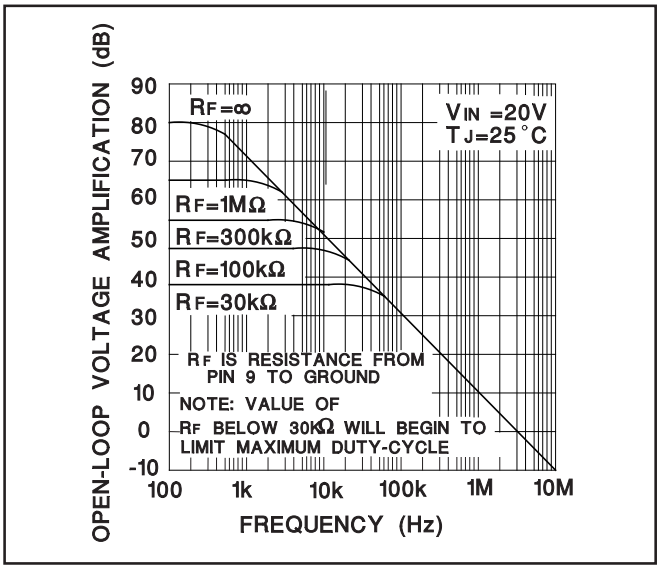
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1524, –25°C to +85°C for the UC2524, and 0°C to +70°C for the UC3524, V_{IN} = 20V, and f = 20kHz, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNITS
		MIN		MAX	MIN		MAX	
Error Amplifier Section (cont.)								
Common Mode Rejection Ratio	T_J = 25°C		70			70		dB
Small Signal Bandwidth	Av = 0dB, T_J = 25°C		3			3		MHz
Output Voltage	T_J = 25°C	0.5		3.8	0.5		3.8	V
Comparator Section								
Duty-Cycle	% Each Output On	0		45	0		45	%
Input Threshold	Zero Duty-Cycle		1			1		V
	Maximum Duty-Cycle		3.5			3.5		V
Input Bias Current			1			1		µA
Current Limiting Section								
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Maximum Out, T_J = 25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.			0.2			0.2		mV/°C
Common Mode Voltage	T_J = –55°C to 85°C for the –1V to 1V Limit	–1		+1	–1		+1	V
	T_J = 125°C	–0.3		+1				V
Output Section (Each Output)								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_{CE} = 40V		0.1	50		0.1	50	µA
Saturation Voltage	Ic = 50mA		1	2		1	2	V
Emitter Output Voltage	V_{IN} = 20V	17	18		17	18		V
Rise Time	Rc = 2kΩ, T_J = 25°C		0.2			0.2		µs
Fall Time	Rc = 2kΩ, T_J = 25°C		0.1			0.1		µs
Total Standby Current (Note)	V_{IN} = 40V		8	10		8	10	mA

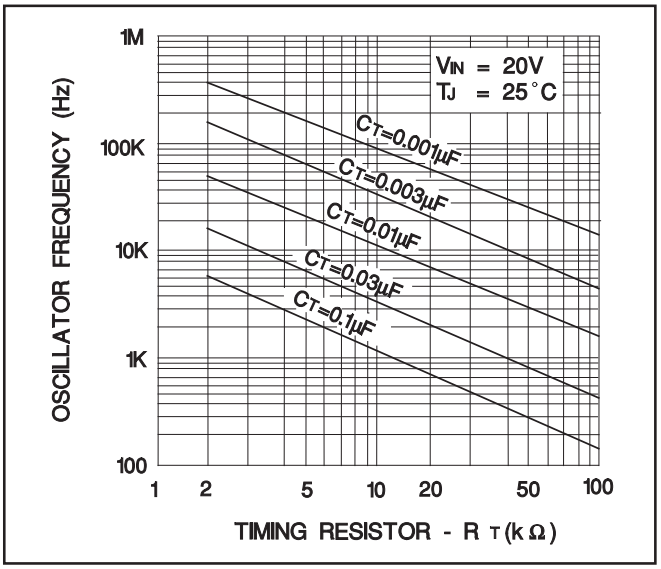
PRINCIPLES OF OPERATION

The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T), and one timing capacitor (C_T), R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q_1 or Q_2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the valve of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier or to provide additional control to the regulator.

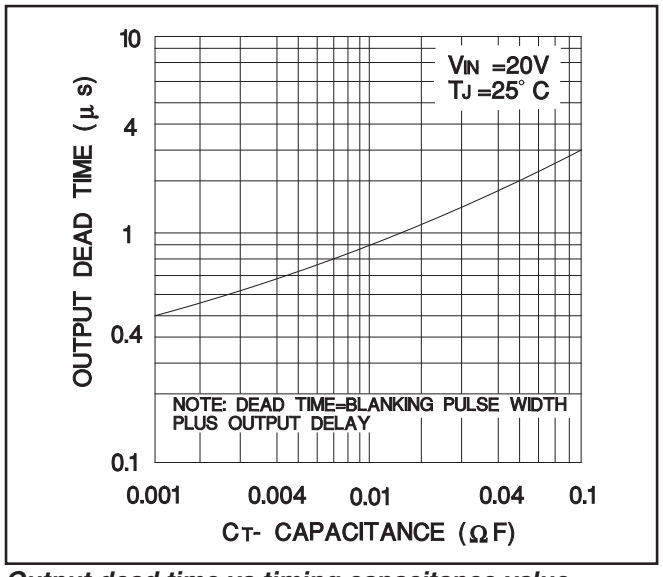
TYPICAL CHARACTERISTICS



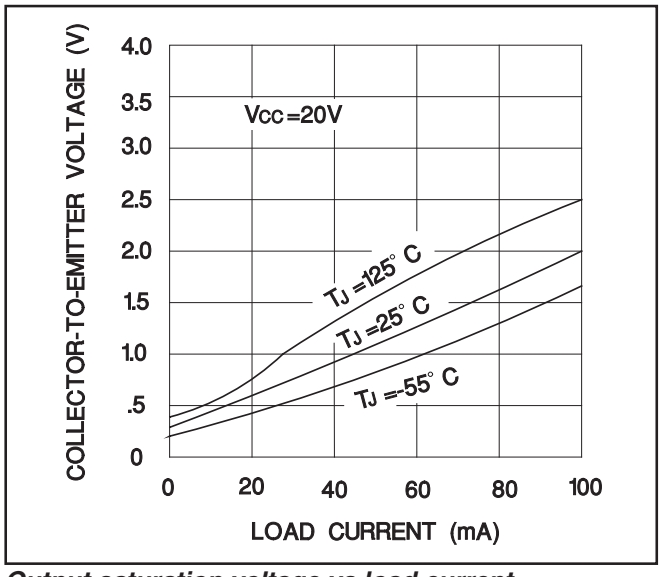
Open-loop voltage amplification of error amplifier vs frequency.



Oscillator frequency vs timing components.



Output dead time vs timing capacitance value.



Output saturation voltage vs load current.

APPLICATION INFORMATION

Oscillator

The oscillator controls the frequency of the UC1524 and is programmed by R_T and C_T according to the approximate formula:

$$f \approx \frac{1.18}{R_T C_T}$$

where R_T is in kΩ
C_T is in mF
f is in kHz

Practical values of C_T fall between 0.001mF and 0.1mF. Practical values of R_T fall between 1.8kΩ and 100kΩ. This results in a frequency range typically from 120Hz to 500kHz.

Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit in Figure 1:

Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2kΩ. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more UC1524 regulators are to operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to single timing capacitor, and the timing resistor connected to a single R_T, terminal.

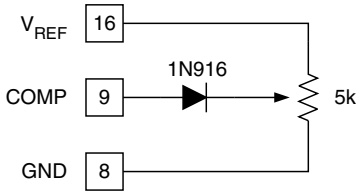


Figure 1. Error amplifier clamp.

The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between the C_T terminals.

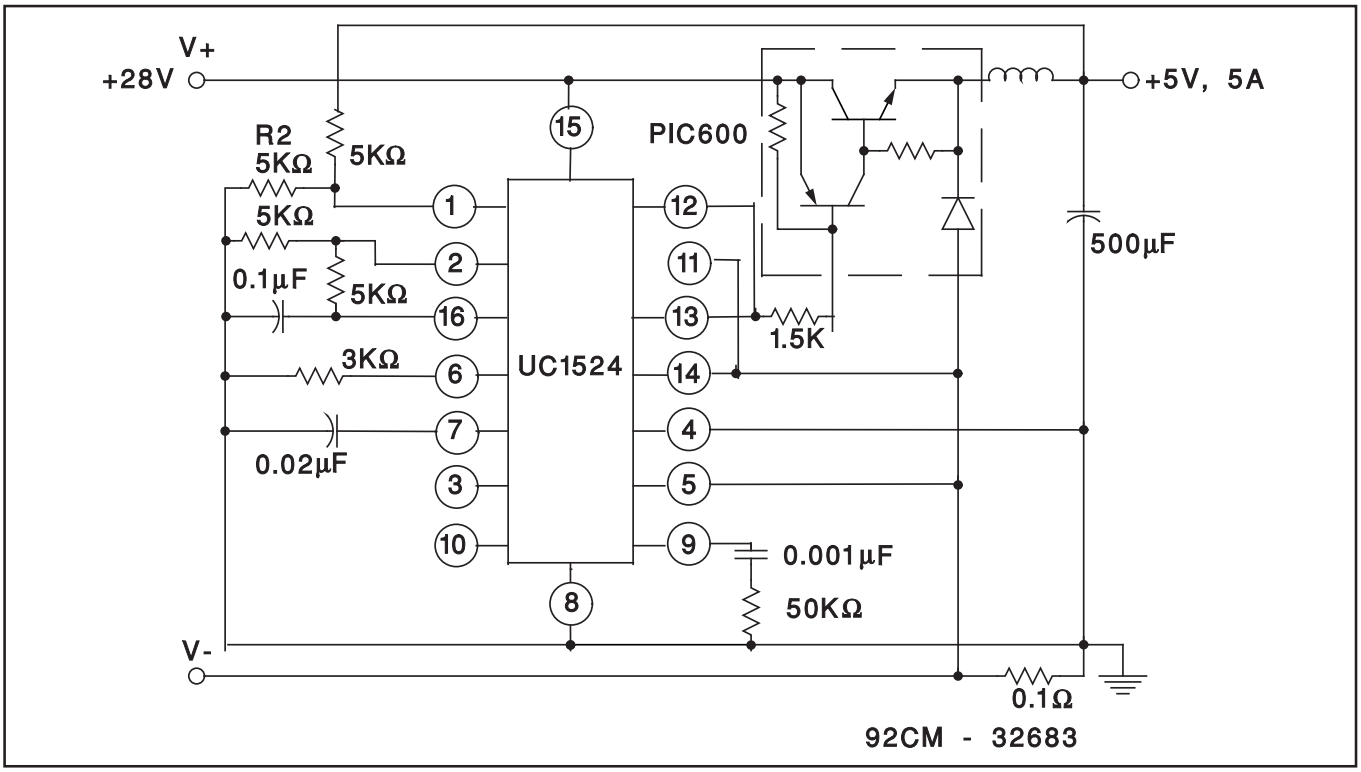


Figure 2. Single-ended LC switching regulator circuit.

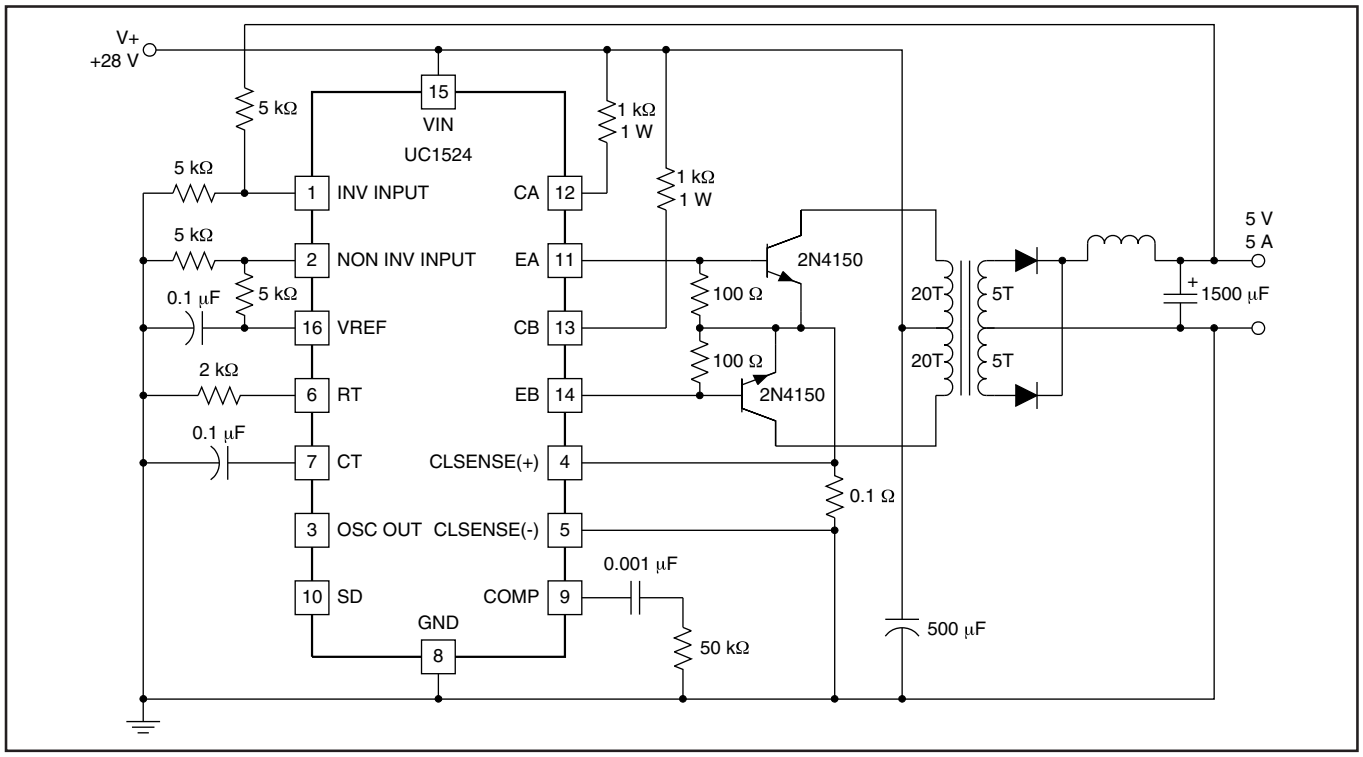


Figure 3. Push-pull transformer coupled circuit.

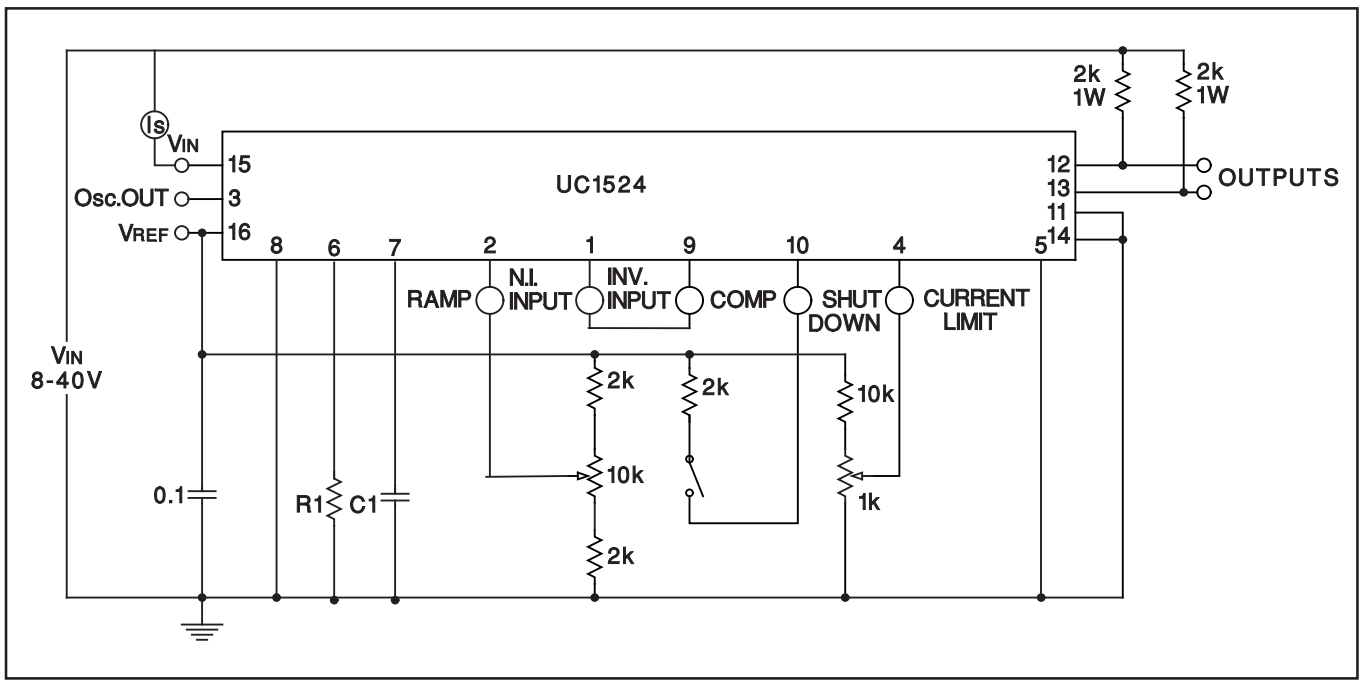


Figure 4. Open loop test circuit.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UC1524J	OBSOLETE	CDIP	J	16		None	Call TI	Call TI
UC1524J/80937	OBSOLETE	CDIP	J	16		None	Call TI	Call TI
UC1524J883B	OBSOLETE	CDIP	J	16		None	Call TI	Call TI
UC2524DW	ACTIVE	SOIC	DW	16	40	None	CU NIPDAU	Level-2-220C-1 YEAR
UC2524DWTR	ACTIVE	SOIC	DW	16	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
UC2524J	OBSOLETE	CDIP	J	16		None	Call TI	Call TI
UC2524N	ACTIVE	PDIP	N	16	25	None	CU SNPB	Level-NA-NA-NA
UC3524D	ACTIVE	SOIC	D	16	40	None	CU NIPDAU	Level-1-220C-UNLIM
UC3524DTR	ACTIVE	SOIC	D	16	2500	None	CU NIPDAU	Level-1-220C-UNLIM
UC3524DW	ACTIVE	SOIC	DW	16	40	None	CU NIPDAU	Level-2-220C-1 YEAR
UC3524DWTR	ACTIVE	SOIC	DW	16	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
UC3524J	OBSOLETE	CDIP	J	16		None	Call TI	Call TI
UC3524N	ACTIVE	PDIP	N	16	25	None	CU SNPB	Level-NA-NA-NA

(1) The marketing status values are defined as follows:
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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