

# MULTI-LOOP DIGITAL CONTROL OF A LINE CONDITIONER USING DPLL

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**Abstract** – This article presents the study of an alternating voltage indirect conditioner, showing the main aspects of its digital control using multiple loop control to regulate and match the output voltage. The objective of this study was to verify the operation of a line conditioner when subjected disturbances, using a digital PLL to generate the reference. The generation of the sinusoidal reference for the output voltage control loop is discussed and digital PLL (DPLL) based on the three-phase instantaneous power theory is proposed. The advantage of the use of a PLL in this work, as a reference, is due to it being immune to variations and disturbances from the mains, being sensitive to the frequency variation that enables the fundamental component of the voltage to be monitored. The conditioner control is based on the concept of multi-loop, one being to control the output voltage RMS value and other for the pre-feeding of the input voltage. Simulation and experimental results obtained with a 3kVA conditioner are presented.

## I. INTRODUCTION

Many environments need regulated voltages with low harmonic distortion, like sensitive loads, laboratories, industrial environments with voltage noise, processing centers and hospitals.

In this work, the indirect voltage conditioner proposed in [2] and studied in [1, 6] was further studied. A variation of the original circuit topology in [3, 7] is proposed. These converters have the advantage of possessing simple commands and they use bidirectional current and unidirectional voltage switches. Thus, the main difference between this topology and others presented in the literature is its simple command circuitry, the use of well-known technologies related to PWM sinusoidal inverters, and the use of switch modules in industrial configurations.

Digital control via Digital Signals Processor (DSPs), besides allowing the use of advanced controlling techniques unthinkable in analog control, eases system monitoring, simplifying the implementation of safety and protection circuits.

The alternating voltage conditioner employing the indirect single-phase ac-ac converter presented in [2] requires a synchronizing signal in phase with the input voltage in order to trigger the switches in the rectifying stage. Moreover, a reference signal, also in phase with the feeding voltage but free of harmonic content must be used for a proper functioning of the converter control.

In [1, 3] the detection of voltage zero crossing moment through a microcontroller to obtain the synchronism signal is used. This technique has an advantage the ease of implementation; however, it can lead to mistakes due to the noise presente in the signal.

DPLL (Digital Phase Locked Loop) systems have been widely used in applications where accurate information on the grid is necessary, such as frequency, angle and phase. Such characteristics become highly attractive to solve the synchronism problem and the reference signal to ac line conditioner. Their implementation can be carried out using a DSP.

The inverter control using current loop, allied to a voltage loop, has been extensively presented in the literature, as [9-10 and 15]. In [11] a technique is presented to avoid the PI controller saturation employed in the control loops.

Loops and pre-feeding are described in [12 and 14] and the concepts of multi-loop, employed in this work, are presented in [12-24 and 16-17].

In the following sections converter operation, reference generation and digital control results, for experimental implementation will be presented.

## II. CONVERTER STRUCTURE AND OPERATION

The simplified circuit of the voltage conditioner is shown in Fig. 1. The switches  $S_1/S_2$  and  $S_3/S_4$  form a bidirectional current rectifier, with low frequency operation, in order to rectify the input voltage. Transformer  $T_1$  has the purpose of applying the output compensation voltage, adding or subtracting from the input voltage. Capacitor  $C_o$  and inductor  $L_o$  form the voltage inverter output filter, which is formed by switches  $S_5/S_6$  and  $S_7/S_8$ . All switches have anti-parallel diodes.

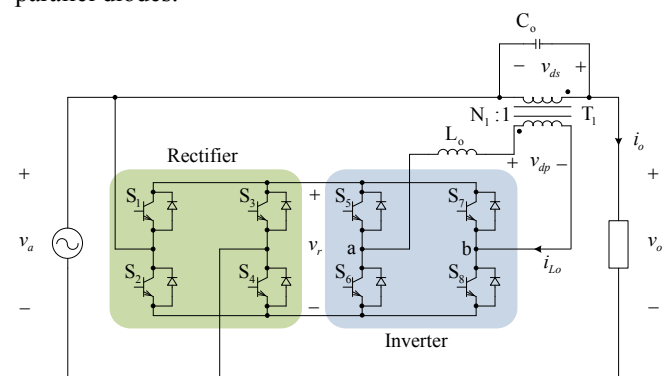


Fig. 1 - Line conditioner circuit.

The rectifier has two operating stages, which are dependent on the ac mains polarity ( $v_i(t)$ ). The full bridge inverter has five operating stages, described in [6]. Filter capacitor  $C_o$  can be positioned on the secondary side of transformer  $T_1$ , using the transformer leakage inductance as an additional output inverter voltage filter. Thus,  $L_o$  represents the total inductance seen by the primary side of the transformer, that is, the leakage plus the inductance of the external inductor.

The circuit of the converter was conceived in order to discard the use of dc link capacitors, but, due to line impedance and parasitic inductances, it is necessary to use a small capacitor, in order to avoid over-voltage across the switches.

In Fig. 2 the duty cycle wave forms for the sinusoidal PWM inverter and for the conditioner are presented. The voltage control represents the behavior of the duty cycle over time. The voltage control for the sinusoidal PWM inverter is a sinusoid, while for the conditioner it is rectangular, therefore it is called a rectangular PWM modulation.

In Fig. 1 and 2 the following variables are shown:

- $v_{ri}(t)$  and  $\overline{v_{ri}}(t)$  - triangular voltages;
- $v_c(t)$  - control voltage;
- $v_{g5,6}(t)$  and  $v_{g7,8}(t)$  - inverter command;
- $v_{ab}(t)$  - inverter output voltage;
- $T_s$  - switching period;
- $d$  - duty cycle;
- $v_{ds}(t)$  - compensation voltage;
- $v_a(t)$  and  $v_o(t)$  - input and output voltages;
- $v_r(t)$  - line-rectified voltage;
- $i_{Lo}(t)$  - filter inductor current.

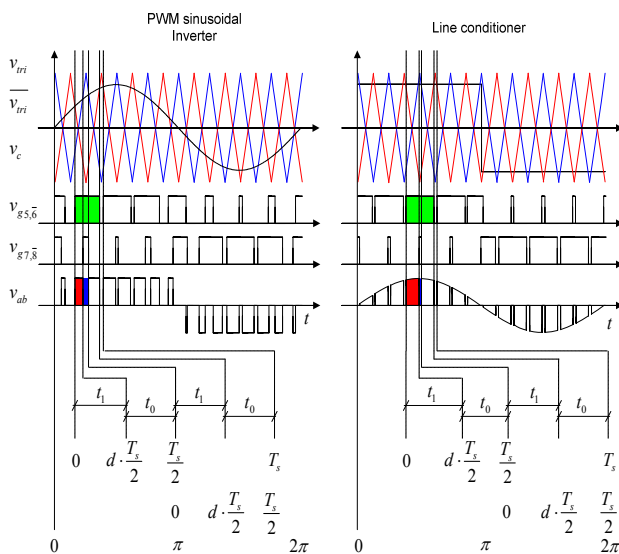


Fig. 2 - Comparison between the modulation of an inverter and a line conditioner.

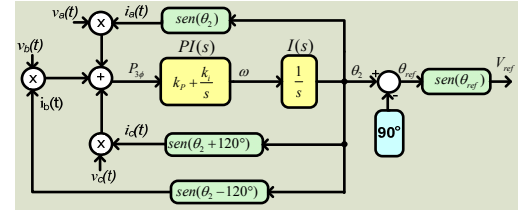


Fig. 3 - Three phase PLL circuit.

### III. GENERATION OF SINUSOIDAL REFERENCE

The correct operation of the line conditioner control system is dependent on the generation of a voltage reference without harmonic content and in phase with the input voltage.

Of the different techniques used to obtain the sinusoidal reference, two of them were studied in a comparative way: detection of voltage zero crossing and through digital PLL.

#### A. Detection of voltage zero crossing

This strategy can be implemented using a microcontroller that has an analog/digital converter to sample the input line voltage. This signal is used in an algorithm that detects the zero crossing moment, synchronizing it with a table of sine values in microcontroller memory. However, reading errors caused by noise presence in the signal sampled are very common, making this technique inexact.

#### B. Digital PLL

A study of three single phase PLL structures is reported in [5], which are differed in terms of the way in which quadrature signal is generated, for instance, inverse Park transformation, Hilbert transformer and using transport delay.

Another strategy for single phase PLL presented in [4] is a simplification of a three-phase structure based in the annulment of dc component of three-phase instantaneous power. This strategy will be used in this work to generate the synchronism signal and the reference that are necessary to the correct behavior of ac line conditioner control.

#### 1) Three-phase PLL circuit.

The three phase PLLs follow the mathematical concept that the sum of the product between two three-phase sinusoidal systems is zero if the phase between both is  $90^\circ$ . Fig. 3 shows a three-phase PLL circuit. The three-phase voltages are acquired starting from the power system, already the three currents are produced internally through sine blocks.

The input phase voltages are:

$$\begin{aligned} v_a(t) &= A \cdot \sin(\theta_1(t)) \\ v_b(t) &= A \cdot \sin(\theta_1(t) - 120^\circ) \\ v_c(t) &= A \cdot \sin(\theta_1(t) + 120^\circ) \end{aligned} \quad (1)$$

Where  $\theta_1$  corresponds to the angle of voltage  $v_a$ . The currents generated internally are presented in (2).

$$\begin{aligned}
i'_a(t) &= B \cdot \sin(\theta_2(t)) \\
i'_b(t) &= B \cdot \sin(\theta_2(t) - 120^\circ) \\
i'_c(t) &= B \cdot \sin(\theta_2(t) + 120^\circ)
\end{aligned} \quad (2)$$

Being  $\theta_2$  the angle of current  $i'_a$ . The three-phase instantaneous power is given by:

$$p'_{3\phi}(t) = v_a(t) \cdot i'_a(t) + v_b(t) \cdot i'_b(t) + v_c(t) \cdot i'_c(t) \quad (3)$$

Substituting (1) and (2) in (3).

$$\begin{aligned}
p'_{3\phi}(t) &= A \cdot B \cdot [\sin(\theta_1(t)) \cdot \sin(\theta_2(t)) + \\
&\sin(\theta_1(t) - 120^\circ) \cdot \sin(\theta_2(t) - 120^\circ) + \\
&\sin(\theta_1(t) + 120^\circ) \cdot \sin(\theta_2(t) + 120^\circ)]
\end{aligned} \quad (4)$$

$$\begin{aligned}
p'_{3\phi}(t) &= \frac{A \cdot B}{2} \cdot [3 \cdot \cos(\theta_1(t) - \theta_2(t)) - \\
&\cos(\theta_1(t) + \theta_2(t)) - \cos(\theta_1(t) + \theta_2(t) + 120^\circ) - \\
&\cos(\theta_1(t) + \theta_2(t) - 120^\circ)]
\end{aligned} \quad (5)$$

Considering the sum of three vectors with same amplitude and  $120^\circ$  shifted is zero, the equation (5) can be simplified by:

$$p'_{3\phi}(t) = \frac{3}{2} \cdot A \cdot B \cdot \cos(\theta_1(t) - \theta_2(t)) \quad (6)$$

Equation (6) shows that when the phase shift between angles  $\theta_1$  and  $\theta_2$  is  $90^\circ$ , the three-phase power is null. This condition is obtained through the PI controller present in Fig. 3.

## 2) Single-phase PLL circuit

For obtaining the single-phased PLL circuit, generated phase voltage and current amplitudes were considered to be unitary. As input value, a phase voltage  $v_a$  is considered, which multiplied by current  $i_a$  generates power  $p_a$ . Rewriting (3):

$$p'_{3\phi} = p_a + p_b + p_c \quad (7)$$

Since  $p_a$  is available in the single-phased PLL circuit, an expression for  $p_b + p_c$  needs to be obtained.

$$p_b + p_c = v_b \cdot i'_b + v_c \cdot i'_c \quad (8)$$

$$\begin{aligned}
p_b + p_c &= \sin(\theta_1 - 120^\circ) \cdot \sin(\theta_2 - 120^\circ) + \\
&\sin(\theta_1 + 120^\circ) \cdot \sin(\theta_2 + 120^\circ)
\end{aligned}$$

$$\begin{aligned}
p_b + p_c &= \frac{1}{2} \cdot [\cos(\theta_1 - \theta_2) - \cos(\theta_1 + \theta_2 + 120^\circ) + \\
&\cos(\theta_1 - \theta_2) - \cos(\theta_1 + \theta_2 - 120^\circ)]
\end{aligned} \quad (9)$$

Knowing that  $\theta_1 = \theta_2 - 90^\circ$ . Expression (9) results in (10):

$$\begin{aligned}
p_b + p_c &= -\frac{1}{2} \cdot [\cos(2\theta_2 + 30^\circ) + \cos(2\theta_2 + 150^\circ)] \\
p_b + p_c &= -\frac{1}{2} \cdot [-\frac{1}{2} \cdot \sin(2\theta_2) - \frac{1}{2} \cdot \sin(2\theta_2)] \\
p_b + p_c &= \frac{1}{2} \sin(2\theta_2)
\end{aligned} \quad (10)$$

Therefore, using (10), the three-phased PLL circuit in Fig. 3, can be simplified to the single-phased circuit shown in Fig. 4.

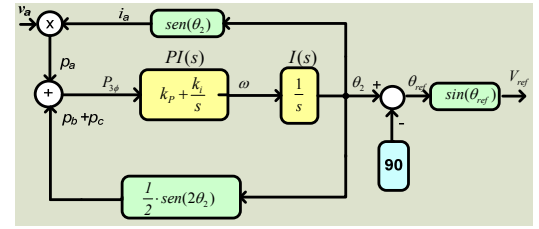


Fig. 4 – Single-phase PLL topology.

## IV. CONDITIONER CONTROL

### A. Topology and Modeling

The controlled converter's block diagram is shown in Fig. 5, where it can be seen that the rectifier's switches ( $S_1/S_2$  and  $S_3/S_4$ ) command is done synchronized with the input voltage, while the inverter's switches ( $S_5/S_6$  and  $S_7/S_8$ ) command is achieved through PWM modulation. The output voltage is controlled instantaneously by a control loop in which the load voltage is compared to a sinusoidal reference and the error signal is compensated by a PID compensator.

The average-current control circuit in the transformer's primary needed to avoid saturation is shown in Fig. 5. This loop compares a sample for the current in the  $T_1$ 's primary and compares it to zero, generating a control signal in order to null the offset voltage in the inverter's output ( $v_{ab}$ ). This control signal is added to the reference voltage ( $v_{res}$ ) and the resulting signal is applied to the voltage compensator ( $C_v(s)$ ).

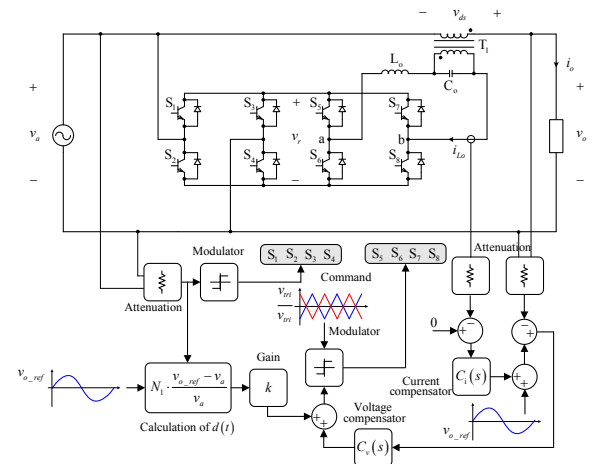


Fig. 5 – Converter control circuit.

For the project of voltage controller ( $C_v(s)$ ) is necessary to determine the transfer functions for the output voltage vs. duty cycle and output voltage vs. input voltage. To model the converter, the following assumptions are made:

- Switches  $S_1$  to  $S_8$  and transformer  $T_1$  are ideal;
- The inductor's and capacitor's equivalent series resistances are negligible;
- The load is purely resistive;
- The commutation frequency ( $\omega_s = 2\pi F_s$ ) is much greater than the ac mains frequency ( $\omega_r = 2\pi F_r$ ).

Since the inverter is a Buck type converter, operating with three-level modulation, it can be modeled as a dc-dc circuit, with the maximum ac mains voltage, using Vorpérian's

PWM switch model as is shown in Fig. 6. Beginning from these circuit expressions (13) and (14) can be obtained.

Bode diagrams of expression (13) are similar to buck and forward dc-dc converters as well known in the literature. A PID (proportional-integral-derivative) controller allows obtaining good results in closed loop operation, for a system with transfer functions given by (13) and (14). Expressions (11) and (12) are valid for the converter presented in Fig. 5, independent of the type of control employed. They represent respectively the transforming ratio in  $T_1$  and the static gain.

$$n_1 = \frac{v_{dp}(t)}{v_{ds}(t)} = \frac{1-\Delta}{\Delta} \cdot D_{max} \quad (11)$$

$$g(t) = \frac{v_o(t)}{v_a(t)} = \frac{n_1 + d(t)}{n_1} \quad (12)$$

$$G(s) = \left. \frac{\hat{v}_o}{\hat{d}} \right|_{\hat{v}_a=0} = \frac{V_a \cdot R_o \cdot n_1}{s^2 \cdot L_o \cdot C_o \cdot R_o + s \cdot L_o + R_o \cdot n_1^2} \quad (13)$$

$$F(s) = \left. \frac{\hat{v}_o}{\hat{v}_a} \right|_{\hat{d}=0} = \frac{R_o \cdot (s^2 \cdot L_o \cdot C_o + n_1^2 + n_1 \cdot D)}{s^2 \cdot L_o \cdot C_o \cdot R_o + s \cdot L_o + R_o \cdot n_1^2} \quad (14)$$

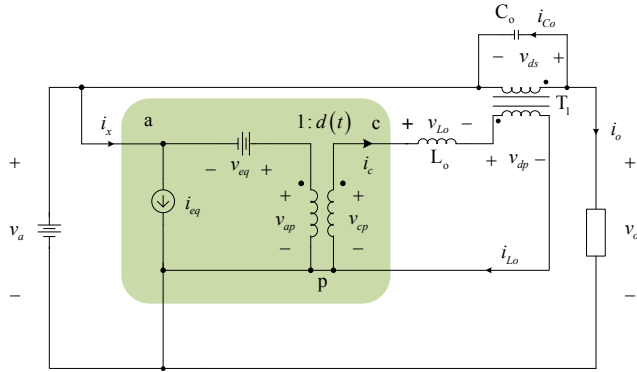


Fig. 6 - Equivalent circuit for small signal model.

With the line impedance and the input filter, the complexity of  $G(s)$  mounts and control becomes more difficult [1].

Beside that, the presence of line impedances creates zeros in the transfer function  $G(s)$  placed in the right-hand side of the complex plane, making it a non-minimal-phase. A more detailed explanation of this problem can be found in [1].

If an input filter is not used, the converter's dynamic response should be slow in order not to be unstable. The use of input filters makes possible the use of fast controllers, keeping in mind the parametric variations in the plant's parameters such as line impedance, load, and operation points among others.

### B. Digital Control

The DSP used in the ac line conditioner was the *Texas Instruments*' TMS320LF2407A. In it, all the converter's control is done, in order to obtain the signals for the switches  $S_5$  to  $S_8$ , besides generating the voltage reference, which is obtained through the PLL system presented in Fig. 4. The control signals for the rectifier ( $S_1$  to  $S_4$ ) was

obtained using analogical comparators.

The control system implemented for the voltage conditioner in the DSP is shown in Fig. 7. The algorithm related to the PLL system has as its input the voltage  $v_{a\_DSP}$ , which is generated from the phase voltage  $v_a$ . This voltage, like all others must be attenuated, has the commuting noise filtered and added by a continuous component in order to eliminate negative values.

The signal ( $v_a^*$ ) is applied to the DSP's analog-digital converter and has values between zero and 3.3V. On the output of the algorithm, the reference voltage used in the control and the synchronizing voltage used for triggering rectifier's switches  $S_1$  to  $S_4$  is presented and so is possible the digital control of the rectifier switches, as was made for the inverter switches  $S_5$  to  $S_8$ . It can be seen in Fig. 7 that the proposed digital control.

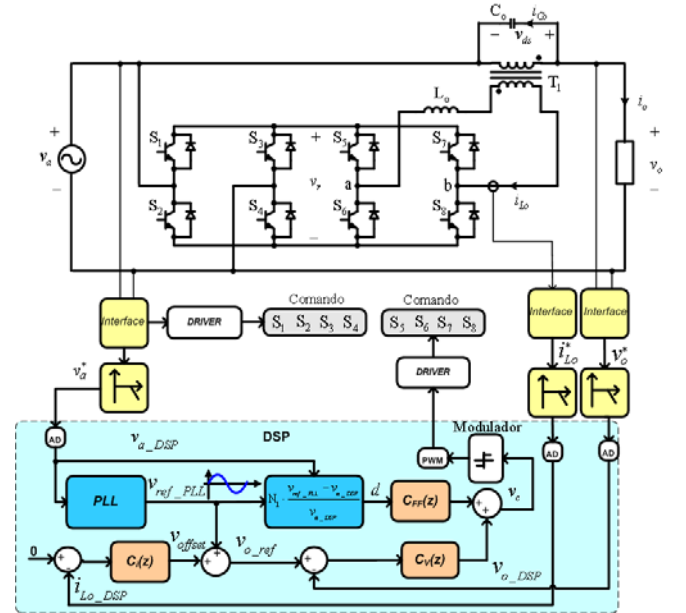


Fig. 7 - Proposed digital control system of line conditioner.

As was explained before, the  $T_1$ 's average primary current compensating voltage is added to the sinusoidal reference generated by the PLL. Compensator ( $C_i(s)$ ) is used to eliminate any average values that the current  $i_{Lo}$  may present. This compensator must have slow dynamics in order not to interfere in the functioning of the output voltage ( $v_o$ ) control loops. Thus, an integrator-type controller was implemented, with a cross over frequency around 1 Hz.

Output voltage control is done by two independent loops, one feedforward and one with effective values. The first aims to generated a control voltage that compensates rapidly variations and distortions present in the input voltage ( $v_a$ ). This loop calculates the duty cycle ( $d$ ) through system variables, isolating  $d$  in (12) as shown by Fig. 5. A low-pass filter was also implemented tuned to a frequency of approximately 1 kHz.

In its turn, the second output voltage control loop has the purpose of minimizing the static error which may be present in  $v_o$ , correcting its effective value. This loop has a first order compensator tuned to a frequency two decades above the value for the current compensator and slower than the feedforward loop in order to prevent interactions between the two loops and converter operating instabilities.



## V. EXPERIMENTAL RESULTS

The conditioner built in the laboratory (Fig.8) has the following specifications:

- $v_a = 220 \pm 20\%[V]$  - input voltage;
- $v_o = 220[V]$  - output voltage;
- $S_o = 3[kVA]$  - output power;
- $F_r = 60[Hz]$  - ac mains frequency;
- $F_s = 20[kHz]$  - commutation frequency;
- $n_1 = 3$  -  $T_1$ 's transforming ratio;
- $L_o = 570[\mu H]$ ,  $C_o = 120[\mu F]$  - output filter.

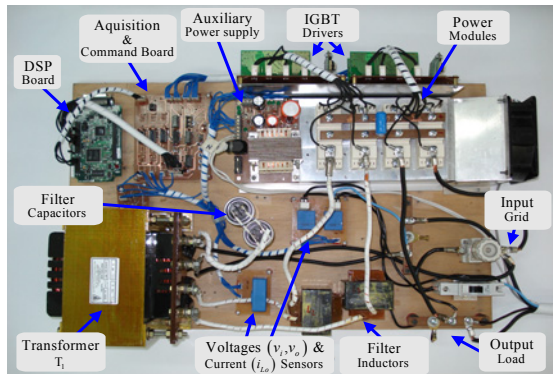


Fig. 8 - Voltage conditioner.

### A. Sinusoidal Reference Generation

In order to verify the PLL circuit shown in Fig. 4 one algorithm was implemented and assembled and two analyses were made from it: the first one use a distorted input voltage and the second one use a square shape voltage as shown in Fig. 9 and Fig. 10 respectively. With the use of blocks of inner memory of DSP, it was stored the variables  $v_a$  and  $v_{ref}$  with objective of visualizing those values, since used DSP doesn't have analog and Digital converter.

Looking at Fig. 10 it seems evident the good operation of the designed PLL even if the input voltage is of a square shape. It can be noticed that after the transient time a sinusoidal with low harmonic content was obtained synchronized and with the same period as the input voltage.

### B. Digital Control

In Fig. 11 a transitory input voltage is shown with the conditioner operating without the feedforward loop. It can be noticed that in region 1 (before the  $v_a$  transient) the input voltage  $v_a$  has an effective value of approximately 210 V,  $v_{ds}$  is in-phase with  $v_a$  and  $v_o$  is 220 V. In region 2 (after the  $v_a$  transient) however,  $v_a$  is changed from 210 V to 240 V, and after a transitory of less than one cycle,  $v_{ds}$  has phase opposite to that of  $v_a$ . The output voltage stays in 220 V.

The same results are presented by Fig. 12, but now with the conditioner operating with the feedforward loop. It can be seen that the dynamic response improved and the output voltage is fast adjusted to its nominal value.

In Fig. 13 and Fig. 14, at no-load operation, the output voltage can be seen when an input voltage with high harmonic content is provided. The first figure shown the results when the conditioner operates without feedforward loop and the second one shows the results with the

feedforward loop. Thanks to the feedforward loop it can be seen the goods results when the output THD is reduced from 4.29% to 3.22%.

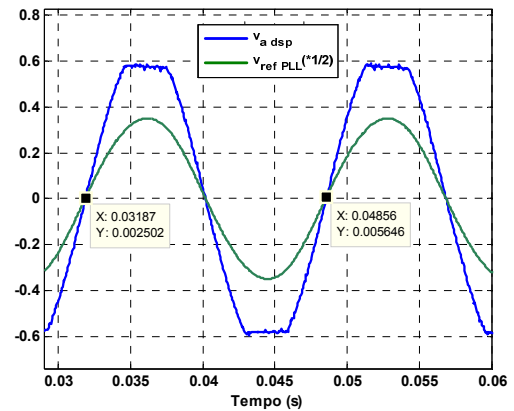


Fig. 9 – PLL system working with distorted input voltage.

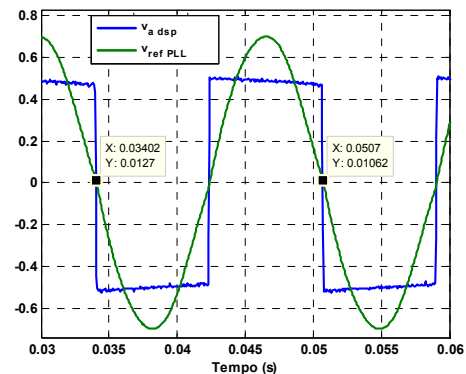


Fig. 10 – PLL system working with square input voltage.

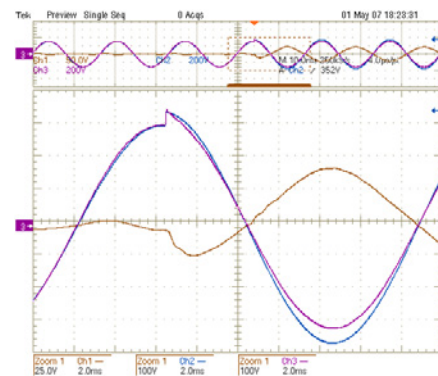


Fig. 11 – Digital control – input voltage transient without feedforward.

In resume, the digital control with the contribution of the PLL system works accordingly other control techniques, like repetitive control, non-linear control state variable based control. Static error is lower than 1% performing a good reference track, but the output voltage THD remains above 3% in contrast with standard suggestions, a clear indication that it must be improved by a careful study of the circuit models and using well tuning controllers.

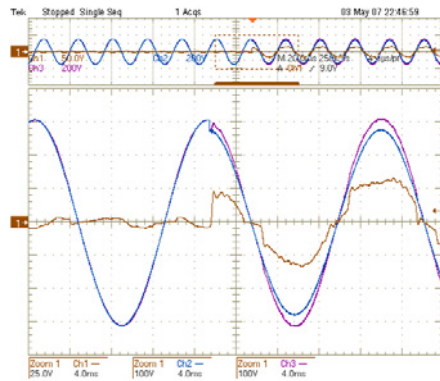


Fig. 12 – Digital control – input voltage transient with feedforward.

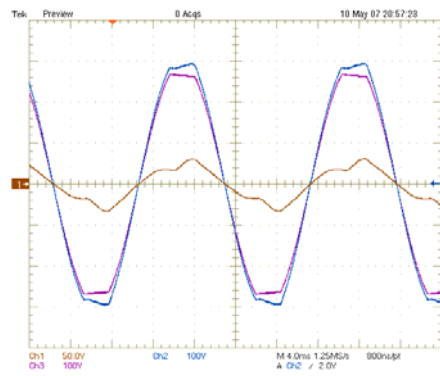


Fig. 13 - Digital control – distorted input voltage without feedforward ( $v_{aTHD}=4.25\%$  and  $v_{oTHD}=4.55\%$  ).

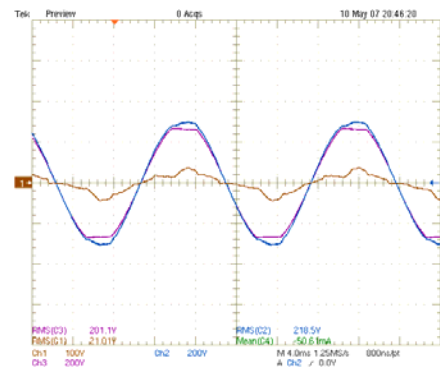


Fig. 14 - Digital control – distorted input voltage with feedforward ( $v_{aTHD}=4.29\%$  and  $v_{oTHD}=3.22\%$  ).

## VI. CONCLUSIONS

In this article the digital control of a 3kVA ac line conditioner was presented. The functioning principles were briefly described. Details of the sinusoidal reference generation were discussed. The system was based on the zero crossing of the main voltage by the theory of active and reactive power using PLL in the digital implementation. The main output voltage control loops were presented, in the digital case with feedforward and effective  $v_o$  control loops. The implemented digital PLL showed an appropriate behavior, even with triangular wave forms, that is, elevated harmonic content. Experimental results showed suitable conditioner behavior operating with distorted input voltage and under  $v_a(t)$  and load variations. The objective was to contribute to the study and implementation of digital PLL algorithms with application in a voltage conditioner.

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