

# Ac Indirect Line Conditioner Digital Control Using PLL Based on the Three-Phase Instantaneous Power Theory

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**Abstract** – This article presents the study of an alternating voltage indirect conditioner, showing the main aspects of its digital and analog control. The generation of the sinusoidal reference for the output voltage control loop is discussed, both in analog and digital control, and for that purpose, a digital PLL based on the three-phase instantaneous power theory is proposed. On the analog controlled converter, an output voltage instantaneous control circuit is used. On the digital control proposed in this work, two circuits are used, one for input voltage feedforward, and one for controlling the effective output voltage. Experimental results obtained with a 10kVA conditioner are presented.

## I. INTRODUCTION

Nowadays, alternating voltage conditioners are frequently used with sensitive loads in home, industry and commerce environments. Their purpose is to provide a regulated voltage, with low harmonic content.

In this work, the indirect voltage conditioner proposed in [2] and studied in [1, 6] is further studied. A variation is proposed to the original circuit topology proposed and studied in [3, 7]. These converters have the advantage of possessing simple command and they use bidirectional current and unidirectional voltage switches.

Digital control via Digital Signals Processor (DSP's), besides allowing the use of advanced controlling techniques unthinkable in analog control, eases system monitoring, simplifying the implementation of safety and protection circuits.

The alternating voltage conditioner employing an indirect single-phased ac-ac converter presented in [2] demands a synchronizing signal in phase with the input voltage in order to trigger the switches in the rectifying stage. Besides that, a reference signal, also in phase with the feeding voltage but free of harmonic content must be used for a proper function of the converter's control.

In [1, 3] is used the detection of voltage zero crossing moment through a microcontroller to get the synchronism signal. This technique has as advantage the easiness in the implementation, however it can cause mistakes due to the noises presence in the signal.

DPLL (Digital Phase Locked Loop) systems have been used broadly in applications where accurately information of the grid is necessary, such as frequency and phase angle is needed. Such characteristic becomes highly attractive to solve the synchronism problem and the reference signal

present at ac line conditioner. Its implementation should be made using a DSP.

In the sequence of this work will be presented: converter operation, reference generation, analog and digital control results for experimental implementation.

## II. CONVERTER STRUCTURE AND OPERATION

The simplified circuit of the voltage conditioner is shown in Fig. 1. The switches  $S_1/S_2$  and  $S_3/S_4$  form a bidirectional current rectifier, with low frequency operation, in order to rectify the input voltage. Transformer  $T_1$  has the purpose of applying the output compensation voltage, adding or subtracting from the input voltage. Capacitor  $C_o$  and inductor  $L_o$  form the voltage inverter's output filter, which is formed by switches  $S_5/S_6$  and  $S_7/S_8$ . All switches have antiparallel diodes.

The rectifier has two operating stages, which depend on the ac mains polarity ( $v_i(t)$ ). The full bridge inverter has five operating stages, described in [6]. Filter capacitor  $C_o$  can be positioned on the secondary side of transformer  $T_1$ , using the transformer's leakage inductance as an additional output inverter voltage filter. So,  $L_o$  represents the total inductance seen by primary side of the transformer, that is, the leakage plus the inductance of the external inductor.

The line impedance, formed by its resistance and inductance, is represented by  $Z_i$ . The converter's circuit was conceived in order to discard the use of dc link capacitors, but, due to line impedance and parasitic inductances, it is necessary to use a small capacitor, in order to avoid overvoltage across the switches.  $Z_f$  and  $Z_a$  represent the conditioner input filter.

In Fig. 2 are presented the duty cycle wave forms for sinusoidal PWM inverter and for the conditioner. The voltage control represents the behavior of duty cycle at the time. The voltage control for sinusoidal PWM inverter is a sinusoid, while for the conditioner is rectangular, then it can be called that rectangular PWM modulation.

In Fig. 1 and 2 the following variables are shown:

- $v_{tri}(t)$  and  $\overline{v_{tri}}(t)$  - triangular voltages;
- $v_c(t)$  - control voltage;
- $v_{g5,6}(t)$  and  $v_{g7,8}(t)$  - inverter's command;
- $v_{ab}(t)$  - inverter's output voltage;

- $T_s$  - switching period;
- $d$  - duty cycle;
- $v_{ds}(t)$  - compensation voltage;
- $v_a(t)$  and  $v_o(t)$  - input and output voltages.

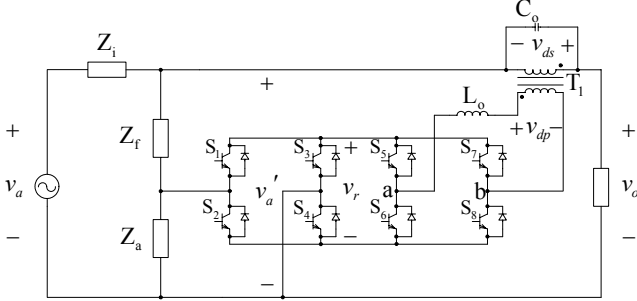


Fig. 1 - Line conditioner circuit.

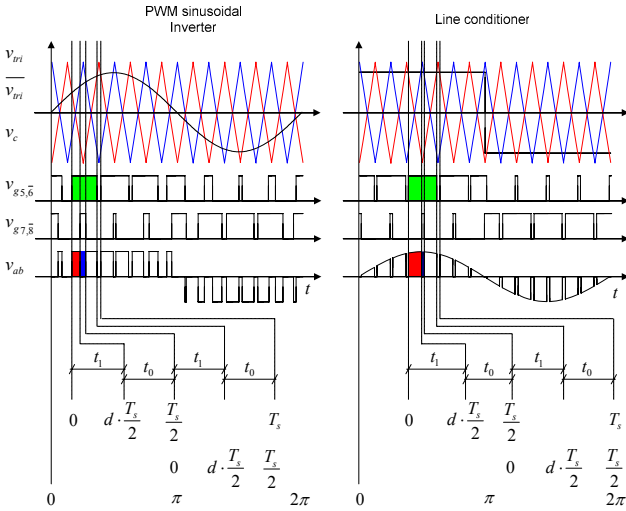


Fig. 2 - Comparison between the modulation of an inverter and a line conditioner.

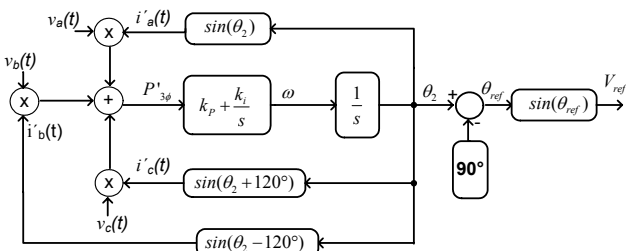


Fig. 3 - Three phase PLL circuit.

### III. GENERATION OF SINUSOIDAL REFERENCE

The correct operation of the line conditioner control system depends on the generation of a voltage reference without harmonic content and in phase with input voltage.

There are two ways to get the sinusoidal reference: detection voltage zero crossing moment and through digital PLL.

#### A. Detection of voltage zero crossing moment

This strategy needs the use of a microcontroller that has an analogical/digital converter to sample the input line voltage. This signal is used in an algorithm that detects the zero crossing moment, synchronizing it with a table of sine values in microcontroller memory. However, errors of reading caused by noises presence in the signal sampled are very common, becoming this technique sufficiently inexact.

#### B. Digital PLL

A study of three single phase PLL structures were presented in [5], which are differed by the way how the quadrature signal is generated, such as, inverse Park transformation, Hilbert transformer and using transport delay.

Another strategy for single phase PLL presented in [4] is a simplification of a three-phase structure based in the annulment of dc component of three-phase instantaneous power. This strategy will be used in this work to generate the synchronism signal and the reference that are necessary to the correct behavior of ac line conditioner control.

##### 1) Three-phase PLL circuit.

The three phase PLLs follow the mathematical concept that the sum of the product between two three-phase sinusoidal systems is zero if the phase between both is 90°. Fig. 3 shows a three-phase PLL circuit. The three-phase voltages are acquired starting from the power system, already the three currents are produced internally through sine blocks.

The input phase voltages are:

$$\begin{aligned} v_a(t) &= A \cdot \sin(\theta_1(t)) \\ v_b(t) &= A \cdot \sin(\theta_1(t) - 120^\circ) \\ v_c(t) &= A \cdot \sin(\theta_1(t) + 120^\circ) \end{aligned} \quad (1)$$

Where  $\theta_1$  corresponds to the angle of voltage  $v_a$ . The currents generated internally are presented in (2).

$$\begin{aligned} i'_a(t) &= B \cdot \sin(\theta_2(t)) \\ i'_b(t) &= B \cdot \sin(\theta_2(t) - 120^\circ) \\ i'_c(t) &= B \cdot \sin(\theta_2(t) + 120^\circ) \end{aligned} \quad (2)$$

Being  $\theta_2$  the angle of current  $i'_a$ . The three-phase instantaneous power is given by:

$$p'_{3\phi}(t) = v_a(t) \cdot i'_a(t) + v_b(t) \cdot i'_b(t) + v_c(t) \cdot i'_c(t) \quad (3)$$

Substituting (1) and (2) in (3).

$$\begin{aligned} p'_{3\phi}(t) &= A \cdot B \cdot [\sin(\theta_1(t)) \cdot \sin(\theta_2(t)) + \\ &\sin(\theta_1(t) - 120^\circ) \cdot \sin(\theta_2(t) - 120^\circ) + \\ &\sin(\theta_1(t) + 120^\circ) \cdot \sin(\theta_2(t) + 120^\circ)] \end{aligned} \quad (4)$$

$$p'_{3\phi}(t) = \frac{A \cdot B}{2} \cdot [3 \cdot \cos(\theta_1(t) - \theta_2(t)) - \cos(\theta_1(t) + \theta_2(t)) - \cos(\theta_1(t) + \theta_2(t) + 120^\circ) - \cos(\theta_1(t) + \theta_2(t) - 120^\circ)] \quad (5)$$

Considering the sum of three vectors with same amplitude and  $120^\circ$  shifted is zero, the equation (5) can be simplified by:

$$p'_{3\phi}(t) = \frac{3}{2} \cdot A \cdot B \cdot \cos(\theta_1(t) - \theta_2(t)) \quad (6)$$

Equation (6) shows that when the phase shift between angles  $\theta_1$  and  $\theta_2$  is  $90^\circ$ , the three-phase power is null. This condition is obtained through the PI controller present in Fig. 3.

### 2) Single-phase PLL circuit

For obtaining the single-phased PLL circuit, generated phase voltage and current amplitudes were considered to be unitary. As input value, a phase voltage  $v_a$  is considered, which multiplied by current  $i_a$  generates power  $p_a$ . Rewriting (3):

$$p'_{3\phi} = p_a + p_b + p_c \quad (7)$$

Since  $p_a$  is available in the single-phased PLL circuit, an expression for  $p_b + p_c$  needs to be obtained.

$$p_b + p_c = v_b \cdot i'_b + v_c \cdot i'_c \quad (8)$$

$$p_b + p_c = \sin(\theta_1 - 120^\circ) \cdot \sin(\theta_2 - 120^\circ) + \sin(\theta_1 + 120^\circ) \cdot \sin(\theta_2 + 120^\circ)$$

$$p_b + p_c = \frac{1}{2} \cdot [\cos(\theta_1 - \theta_2) - \cos(\theta_1 + \theta_2 + 120^\circ) + \cos(\theta_1 - \theta_2) - \cos(\theta_1 + \theta_2 - 120^\circ)] \quad (9)$$

Knowing that  $\theta_1 = \theta_2 - 90^\circ$ . Expression (9) results in (10):

$$p_b + p_c = -\frac{1}{2} \cdot [\cos(2\theta_2 + 30^\circ) + \cos(2\theta_2 + 150^\circ)]$$

$$p_b + p_c = -\frac{1}{2} \cdot [-\frac{1}{2} \cdot \sin(2\theta_2) - \frac{1}{2} \cdot \sin(2\theta_2)]$$

$$p_b + p_c = \frac{1}{2} \sin(2\theta_2) \quad (10)$$

Therefore, using (10), the three-phased PLL circuit in Fig. 3, can be simplified to the single-phased circuit shown in Fig. 4.

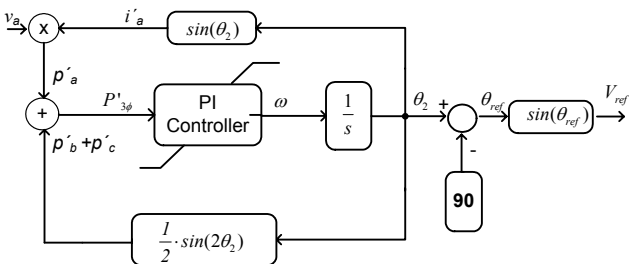


Fig. 4 – Single-phase PLL topology.

## IV. CONDITIONER CONTROL

### A. Analog Control

The analog controlled converter's block diagram is shown in Fig. 5, where it can be seen that the rectifier's switches ( $S_1/S_2$  and  $S_3/S_4$ ) command is done synchronized with the input voltage, while the inverter's switches ( $S_5/S_6$  and  $S_7/S_8$ ) command is achieved through PWM modulation. The output voltage is controlled instantaneously by a control loop in which the load voltage is compared to a sinusoidal reference and the error signal is compensated by a PID compensator.

The average-current control circuit in the transformer's primary needed to avoid saturation is not shown in Fig. 5. This loop compares a sample for the current in the  $T_1$ 's primary and compares it to zero, generating a control signal in order to null the offset voltage in the inverter's output ( $v_{ab}$ ). This control signal is added to the voltage compensator control ( $C(s)$ ) and the resulting signal is applied to the PWM modulator's input.

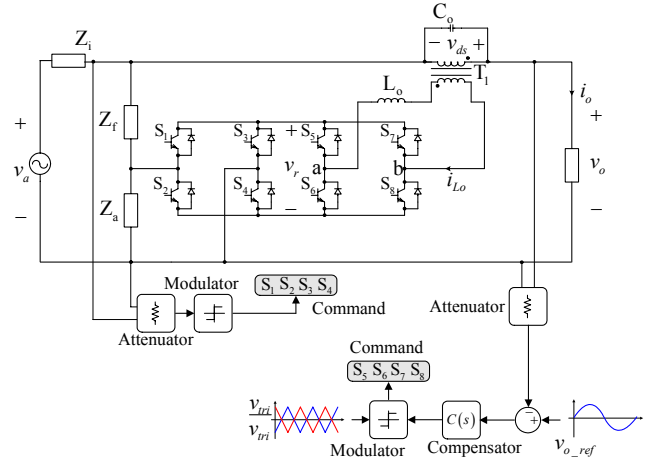


Fig. 5 – Converter analog control circuit.

For the project of voltage controller ( $C(s)$ ) is necessary to determine the transfer functions for the output voltage vs. duty cycle and output voltage vs. input voltage. In Fig. 5,  $Z_i$  is the line impedance,  $Z_f$  and  $Z_a$  are the series and parallel impedances of the input filter, respectively. To model the converter, the following assumptions are made:

- Switches  $S_1$  to  $S_8$  and transformer  $T_1$  are ideal;
- The inductor's and capacitor's equivalent series resistances are negligible;
- The load is purely resistive;
- The commutation frequency ( $\omega_s = 2\pi F_s$ ) is much greater than the ac mains frequency ( $\omega_r = 2\pi F_r$ ).

Since the inverter is a Buck type converter, operating with three-level modulation, it can be modeled as a dc-dc circuit, with the maximum ac mains voltage, using Vorpérian's PWM switch model as is shown in Fig. 6. Beginning from this circuit and eliminating  $Z_i$ ,  $Z_f$  and  $Z_a$ , expressions (13) and (14) can be obtained.

Bode diagrams of expression (13) are similar to buck and forward dc-dc converters as well known in the literature. A PID (proportional-integral-derivative) controller allows

obtaining good results in closed loop operation, for a system with transfer functions given by (13) and (14). Expressions (11) and (12) are valid for the converter presented in Fig. 5, independent of the type of control employed. They represent respectively the transforming ratio in  $T_1$  and the static gain.

$$n_1 = \frac{v_{dp}(t)}{v_{ds}(t)} = \frac{1-\Delta}{\Delta} \cdot D_{max} \quad (11)$$

$$g(t) = \frac{v_o(t)}{v_a(t)} = \frac{n_1 + d(t)}{n_1} \quad (12)$$

$$G(s) = \left. \frac{\hat{v}_o}{\hat{d}} \right|_{\hat{v}_a=0} = \frac{V_a \cdot R_o \cdot n_1}{s^2 \cdot L_o \cdot C_o \cdot R_o + s \cdot L_o + R_o \cdot n_1^2} \quad (13)$$

$$F(s) = \left. \frac{\hat{v}_o}{\hat{v}_a} \right|_{\hat{d}=0} = \frac{R_o \cdot (s^2 \cdot L_o \cdot C_o + n_1^2 + n_1 \cdot D)}{s^2 \cdot L_o \cdot C_o \cdot R_o + s \cdot L_o + R_o \cdot n_1^2} \quad (14)$$

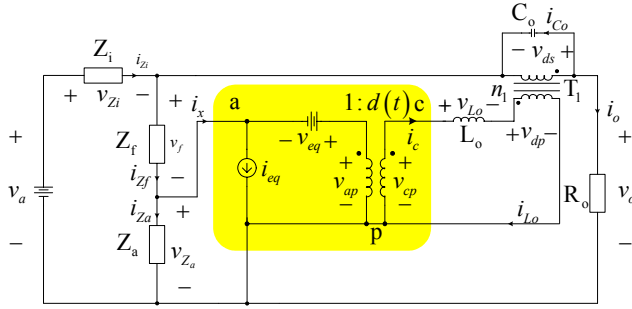


Fig. 6 - Equivalent circuit for small signal model.

With the line impedance and the input filter, the complexity of  $G(s)$  mounts and control becomes more difficult.

Beside that, the presence of line impedances creates zeros in the transfer function  $G(s)$  placed in the right-hand side of the complex plane, making it a non-minimal-phase. A more detailed explanation of this problem can be found in [1].

If an input filter is not used, the converter's dynamic response should be slow in order not to be unstable. The use of input filters makes possible the use of fast controllers, keeping in mind the parametric variations in the plant's parameters such as line impedance, load, operation points among others.

### B. Digital Control

The DSP used in the ac line conditioner was the *Texas Instruments' TMS320LF2407A*. In it, all the converter's control is done, in order to obtain the signals for the switches  $S_1$  to  $S_8$ , besides generating the voltage reference, which is obtained through the PLL system presented in Fig. 4.

The control system implemented for the voltage conditioner in the DSP is shown in Fig. 7. The algorithm related to the PLL system has as its input the voltage  $v_a^*_{-DSP}$ , which is generated from the phase voltage  $v_a$ . This voltage, like all others must be attenuated, have the commuting noise

filtered and added by a continuous component in order to eliminate negative values.

The signal ( $v_a^*$ ) is applied to the DSP's analog-digital converter and has values between zero and 3.3V. On the output of the algorithm, the reference voltage used in the control and the synchronizing voltage used for triggering rectifier's switches  $S_1$  to  $S_4$ , is presented.

It can be seen in Fig. 7 that the proposed digital control system is significantly different from the analog one presented previously. On the first, only the control loops for average transformer's primary current instantaneous output voltage were implemented.

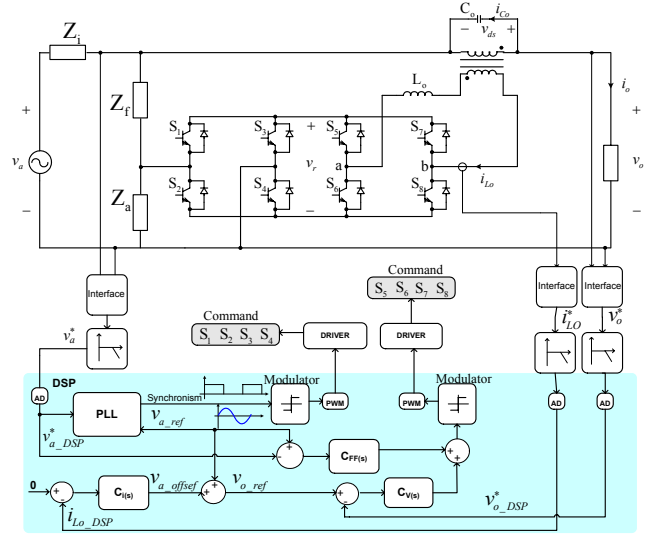


Fig. 7 - Proposed digital control system of line conditioner.

The  $T_1$ 's average primary current compensating voltage is added to the sinusoidal reference generated by the PLL. Compensator ( $C_i(s)$ ) is used to eliminate any average values that the current  $i_{Lo}$  may present. This compensator must have slow dynamics in order not to interfere in the functioning of the output voltage ( $v_o$ ) control loops. Thus, an integrator-type controller was implemented, with a cross over frequency around 1 Hz.

Output voltage control is done by two independent loops, one *feedforward* and one with effective values. The first aims to generated a control voltage that compensates rapidly variations and distortions present in the input voltage ( $v_a$ ). This loop calculates the duty cycle ( $d$ ) through system variables, isolating  $d$  in (12). A low-pass filter was also implemented tuned to a frequency of approximately 1 kHz.

In its turn, the second output voltage control loop has the purpose of minimizing the static error which may be present in  $v_o$ , correcting its effective value. This loop has a first order compensator tuned to a frequency two decades above the value for the current compensator.

## V. EXPERIMENTAL RESULTS

The conditioner built in the laboratory (Fig. 8) has the following specifications:

- $v_a = 220 \pm 20\%[V]$  - input voltage;

- $v_o = 220[V]$  - output voltage;
- $S_o = 10[kVA]$  - output power;
- $F_r = 60[Hz]$  - ac mains frequency;
- $F_s = 20[kHz]$  - commutation frequency;
- $n_1 = 3$  -  $T_1$ 's transforming ratio;
- $L_o = 570[\mu H]$ ,  $C_o = 120[\mu F]$  - output filter;
- $L_f = 100[\mu H]$ ,  $C_{f1} = 60[\mu F]$ ,  $R_{f1} = 1[\Omega]$   
 $C_{f2} = 10[\mu F]$ ,  $R_{f2} = 1.2[\Omega]$  - input filter.

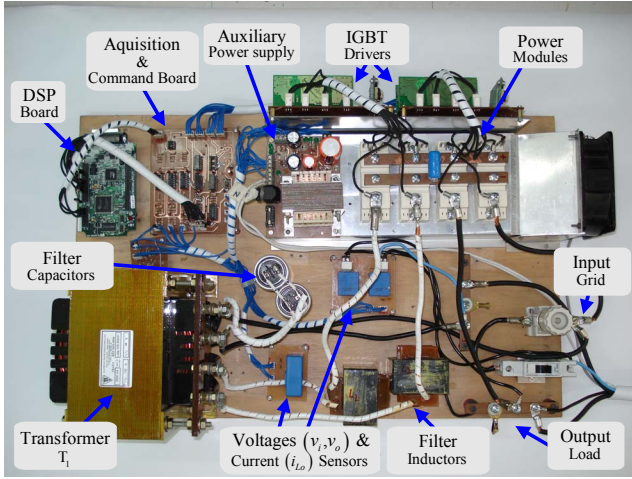


Fig. 8 - Voltage conditioner.

#### A. Sinusoidal Reference Generation

In order to verify the PLL circuit shown in Fig. 4 one algorithm was implemented and assembled and two analyses were made from it: the first use a sinusoidal input voltage and the second use a triangular shape voltage as shown in Fig. 9 and Fig. 10 respectively. With the use of blocks of inner memory of DSP, it was stored the variables  $v_a$  and  $v_{ref}$  with objective of visualizing those values, since used DSP doesn't have analog and Digital converter.

Looking at Fig. 10 it seems evident the good operation of the designed PLL even if the input voltage is of a triangular shape. It can be noticed that after the transient time a sinusoidal with low harmonic content was obtained synchronized and with the same period as the input voltage.

#### B. Analogical Control

The experimental results obtained for the previous design prototype are shown by Fig. 11 and Fig. 12 in which an input voltage and load perturbation was applied. Fig. 11 shows the output voltage behavior with and without input filter.

#### C. Digital Control

In the voltage conditioner with digital control the input filter was not used. In Fig. 14, at no-load operation, the

output voltage can be seen when an input voltage with high harmonic content is provided. In Fig. 13 a transitory input voltage is shown. It can be noticed that in region 1 the input voltage  $v_a$  has an effective value of approximately 210 V,  $v_{ds}$  is in-phase with  $v_a$  and  $v_o$  is 220 V. In region 2 however,  $v_a$  is changed from 210 V to 240 V, and after a transitory of less than one cycle,  $v_{ds}$  has phase opposite to that of  $v_a$ . The output voltage stays in 220 V.

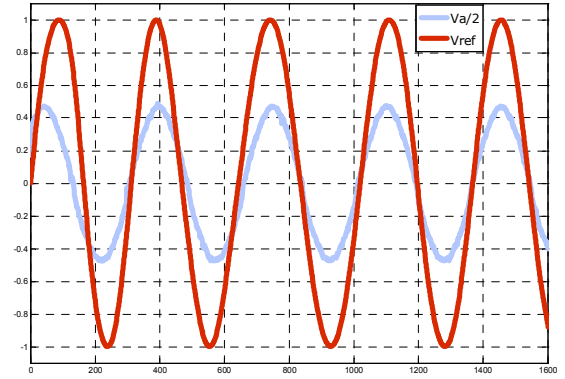


Fig. 9 – PLL system working with sinusoidal input voltage.

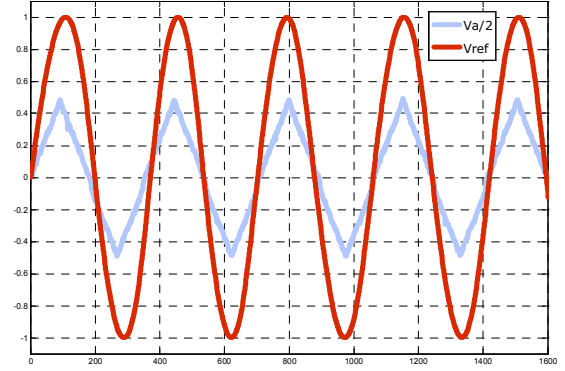


Fig. 10 – PLL system working with triangular input voltage.

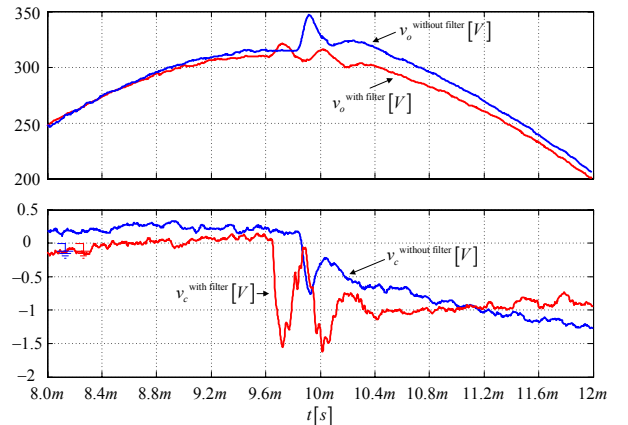


Fig. 11 – Analogical control - +10% input voltage transient.

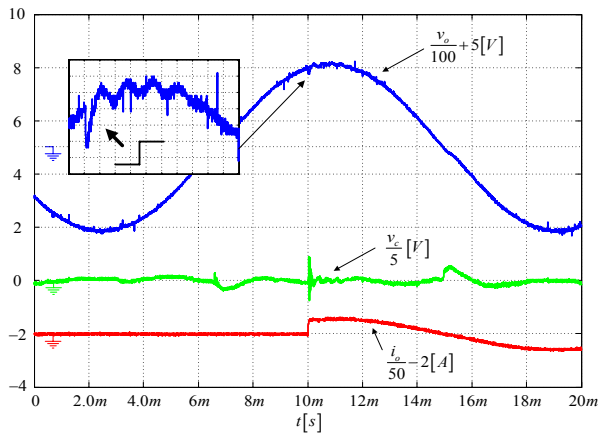


Fig. 12 – Analogical control - 50% load transient.

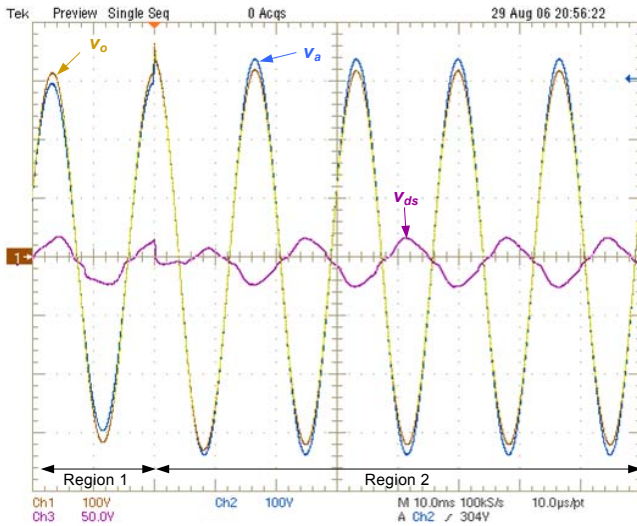


Fig. 13 – Digital control – input voltage transient.

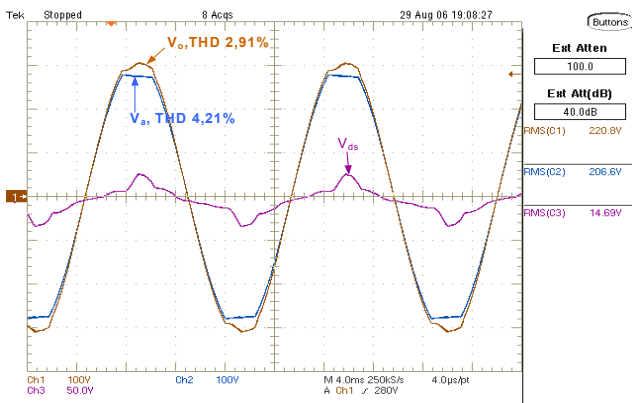


Fig. 14 - Operation with THD of 4,21% in input voltage

## VI. CONCLUSIONS

In this article, analog and digital control of a 10kVA ac line conditioner is presented. The functioning principles were presented briefly

Details of the sinusoidal reference generation were discussed. The system was based on the passage by zero of the network voltage for the analog implementation, and in the theory of active and reactive power using PLL in the digital implementation.

The main output voltage control loops were presented, in the analog case with instantaneous values, and in the digital case with feedforward and effective  $v_o$  control loops.

The implemented digital PLL presented an adequate behavior, even with triangular wave forms, that is, elevated harmonic content.

Experimental results show an appropriate conditioner's behavior operating with distorted input voltage and under  $v_a$  and load variations.

## VII. ACKNOWLEDGMENT

The authors would like to thank CAPES for the financial support.

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