Digital Control Based on DPLL of an AC Line Conditioner

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***Abstract*—The goal of this work is to accomplish a study and design an indirect voltage conditioner controlled digitally through digital signal processor (DSP) based on digital PLL (Phase Locked Loop). A digital PLL (DPLL) is proposed and implemented using the three-phase instantaneous power theory. The PLL used as reference signal does not contain harmonic distortions, and follows frequency variations in the power supply. The advantage of using PLL as reference lies in the immunity to variations and disturbances of the mains, besides being sensitive to the frequency variation, which make possible to follow the fundamental component of the voltage. For the digital control proposed in this work, two loops are used, one for input voltage feedforward, and the other one for controlling the effective output voltage. With the use of DSP, all the control algorithms can be developed in assembly language. Simulation and experimental results obtained on a 3 kVA conditioner are also presented. The ac-ac indirect conditioner does not use a dc link, as its weight and cost is reduced if compared with classical back-to-back topologies.**

I. INTRODUCTION

Voltage conditioners are frequently used with sensitive loads in home, industry, and commerce environments. Their purpose is to provide regulated voltage, with low harmonic content [8-10]. In this work, the indirect voltage conditioner proposed in [2] and studied in [1, 6] is further studied. A variation is proposed to the original topology proposed and studied in [3, 7]. These converters have the advantages of simple command and using bidirectional current and unidirectional voltage switches. Digital control via Digital Signals Processors (DSPs), besides allowing the use of advanced control techniques unthinkable to analog control, simplifies system monitoring and also the implementation of safety and protection circuits [12-14]. The voltage conditioner employing an indirect single-phase ac-ac converter presented in [2] demands a synchronizing signal in phase with the input voltage in order to drive the switches in the rectifier stage. Besides that, a reference signal, also in phase with the supply voltage but free of harmonic content, must be used for the accurate operation of the converter.

DPLL (Digital Phase Locked Loop) systems have been widely used in applications where accurate information acquired from the grid is necessary, such as frequency, angle, and phase. Such characteristic becomes highly attractive to solve the synchronism issue and provides the reference signal present in ac line conditioners.

II. CONVERTER STRUCTURE AND OPERATION

The simplified circuit of the voltage conditioner is shown in Fig. 1. Switches S_1/S_2 and S_3/S_4 constitute a bidirectional current rectifier operating at low frequency in order to rectify the input voltage. Transformer T_1 has the purpose of applying the output compensation voltage, adding or subtracting it from the input voltage. Capacitor C_o and inductor L_o are the output filter elements of the voltage inverter, which is formed by switches S_5/S_6 and S_7/S_8. It must be also mentioned that all switches have antiparallel diodes. The rectifier has two operating stages, which depend on the ac mains polarity ($v_i(t)$). The full-bridge inverter has five operating stages, described in [6]. Filter capacitor C_o can be placed on the secondary side of transformer T_1, using the transformer leakage inductance as an additional output voltage filter. Therefore L_o represents the total inductance seen from the primary side of the transformer, that is, the leakage inductance plus that of the external inductor.

The converter circuit is implemented in order to discard the use of dc link capacitors, but due to line impedance and parasitic inductances, it is necessary to use a small capacitor to avoid overvoltage across the switches. In Fig. 2, the duty cycle waveforms for sinusoidal PWM inverter and the conditioner are presented The voltage control represents the behavior of duty cycle at this instant. The voltage control for the PWM inverter is a sinusoid, while that of the conditioner is rectangular, and so it can be called rectangular PWM modulation. The following variables are shown in Fig. 1 and Fig. 2: $v_{tri}(t)$ and $\overline{v_{tri}}(t)$ are triangular voltages; $v_c(t)$ is the control voltage; $v_{g5,6}(t)$ and $v_{g7,8}(t)$ are the drive signals of the inverter switches; $v_{ab}(t)$ is the inverter output voltage; T_s is the switching period; d is the duty cycle; $v_{ds}(t)$ is the compensation voltage; and $v_a(t)$ and $v_o(t)$are the input and output voltages, respectively.

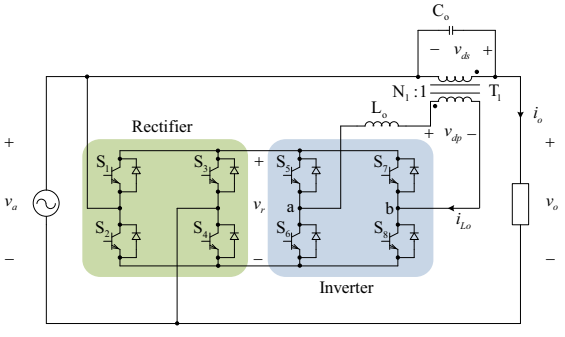

Figure 1. Line conditioner circuit with the ac-ac converter connected to the line.

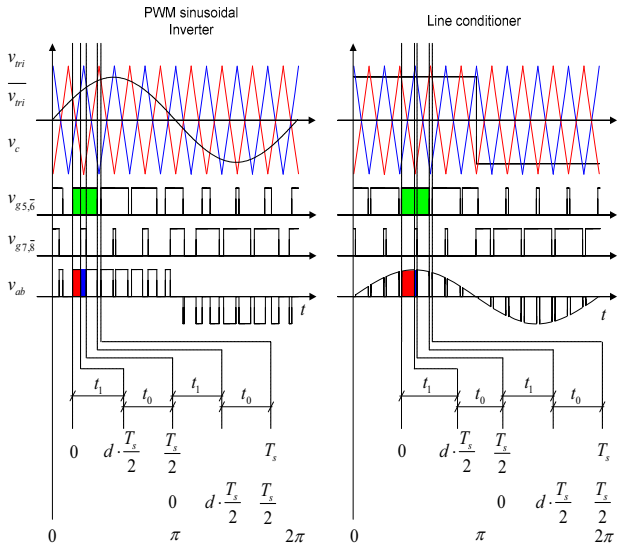

Figure 2. Comparison between the modulation of an inverter and a line conditioner.

III. GENERATION OF SINUSOIDAL REFERENCE

The accurate operation of the line conditioner control system depends on the generation of a voltage reference without harmonic content and in phase with the input voltage. There are many ways to obtain the sinusoidal reference, for instance, detection of the voltage zero crossing instant and through digital PLL (DPLL). The latter method is employed in this work to accomplish this task.

A. Detection of voltage zero crossing instant

This strategy demands the use of a microcontroller that has an analog-to-digital converter to sample the input line voltage. This signal is used in an algorithm that detects the zero crossing instant, synchronizing it with a table of sine values in microcontroller memory. However, reading errors caused by the presence of noise in the sampled signal are very common, and thus this technique may not be sufficiently accurate.

B. Digital PLL

A study of three single-phase PLL structures are presented in [5], which are distinguished by the way the quadrature signal is generated, such as inverse Park transformation, Hilbert transformer and use of transport delay.

Another strategy for single-phase PLL presented in [4] is the simplification of a three-phase structure based on the elimination of the dc component of three-phase instantaneous power. This strategy will be used in this work to generate the synchronism signal and the reference that are necessary to guarantee the accurate behavior of the ac line conditioner control.

1) Three-phase PLL circuit.

Three phase PLLs follow the mathematical concept that the sum of the product between two three-phase sinusoidal systems is zero if the phase between both them is 90°. Fig. 3 shows a three-phase PLL circuit. The three-phase voltages are acquired from the power system, as the three currents are generated internally through sine blocks.

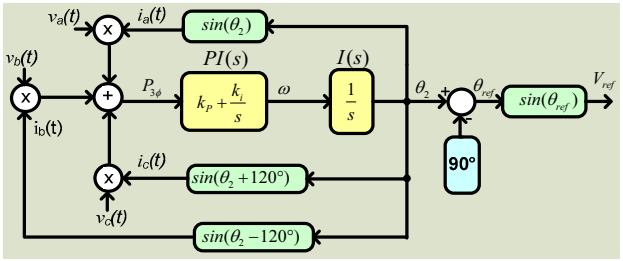

Figure 3. Three-phase PLL circuit.

The input phase voltages are:

$$\begin{aligned} v_a(t) &= A\cdot\sin\left(\theta_1(t)\right) \\ v_b(t) &= A\cdot\sin\left(\theta_1(t)-120°\right) \\ v_c(t) &= A\cdot\sin\left(\theta_1(t)+120°\right) \end{aligned} \quad (1)$$

Where θ_1 corresponds to the phase of voltage v_a. The currents generated internally are presented in (2).

$$\begin{aligned} i'_a(t) &= B\cdot\sin\left(\theta_2(t)\right) \\ i'_b(t) &= B\cdot\sin\left(\theta_2(t)-120°\right) \\ i'_c(t) &= B\cdot\sin\left(\theta_2(t)+120°\right) \end{aligned} \quad (2)$$

Being θ_2 the phase of current i_a'. The three-phase instantaneous power is given by:

$$p'_{3\phi}(t) = v_a(t)\cdot i'_a(t) + v_b(t)\cdot i'_b(t) + v_c(t)\cdot i'_c(t) \quad (3)$$

Substituting (1) and (2) in (3) gives:

$$\begin{aligned} p'_{3\phi}(t) = A\cdot B\cdot[&\sin\left(\theta_1(t)\right)\cdot\sin\left(\theta_2(t)\right)+ \\ &\sin\left(\theta_1(t)-120°\right)\cdot\sin\left(\theta_2(t)-120°\right)+ \\ &\sin\left(\theta_1(t)+120°\right)\cdot\sin\left(\theta_2(t)+120°\right)] \end{aligned} \quad (4)$$

$$\begin{aligned} p'_{3\phi}(t) = \frac{A\cdot B}{2}\cdot[&3\cdot\cos\left(\theta_1(t)-\theta_2(t)\right)- \\ &\cos\left(\theta_1(t)+\theta_2(t)\right)-\cos\left(\theta_1(t)+\theta_2(t)+120°\right) \\ &-\cos\left(\theta_1(t)+\theta_2(t)-120°\right)] \end{aligned} \quad (5)$$

Considering that the sum of three vectors with same amplitude and 120° shifted is zero, equation (5) can be simplified as:

$$p'_{3\phi}(t) = \frac{3}{2}\cdot A\cdot B\cdot\cos\left(\theta_1(t)-\theta_2(t)\right) \quad (6)$$

Equation (6) shows that when the phase shift between angles θ_1 and θ_2 is 90°, the three-phase power is null. This condition is obtained through the PI controller presented in Fig. 3.

2) Single-phase PLL circuit

To obtain the single-phase PLL circuit, generated phase voltage and current amplitudes are considered to be unity. As input value, phase voltage v_a is considered, which multiplied by current i_a generates power p_a. Rewriting (3):

$$p'_{3\phi} = p_a + p_b + p_c \quad (7)$$

Since p_a is available in the single-phase PLL circuit, an expression for p_b+p_c needs to be obtained.

$$p_b + p_c = v_b \cdot i'_b + v_c \cdot i'_c \tag{8}$$

$$p_b + p_c = \sin(\theta_1 - 120°) \cdot \sin(\theta_2 - 120°) + \sin(\theta_1 + 120°) \cdot \sin(\theta_2 + 120°)$$

$$p_b + p_c = \tfrac{1}{2} \cdot [\cos(\theta_1 - \theta_2) - \cos(\theta_1 + \theta_2 + 120°) + \cos(\theta_1 - \theta_2) - \cos(\theta_1 + \theta_2 - 120°)] \tag{9}$$

Knowing that $\theta_1=\theta_2$-90°, expression (9) results in (10):

$$p_b + p_c = -\tfrac{1}{2} \cdot [\cos(2\theta_2 + 30°) + \cos(2\theta_2 + 150°)]$$

$$p_b + p_c = -\tfrac{1}{2} \cdot [-\tfrac{1}{2} \cdot \sin(2\theta_2) - \tfrac{1}{2} \cdot \sin(2\theta_2)]$$

$$p_b + p_c = \tfrac{1}{2} \sin(2\theta_2) \tag{10}$$

Therefore, using (10), the three-phase PLL circuit in Fig. 3 can be simplified to the single-phase circuit shown in Fig. 4 and Fig. 5.

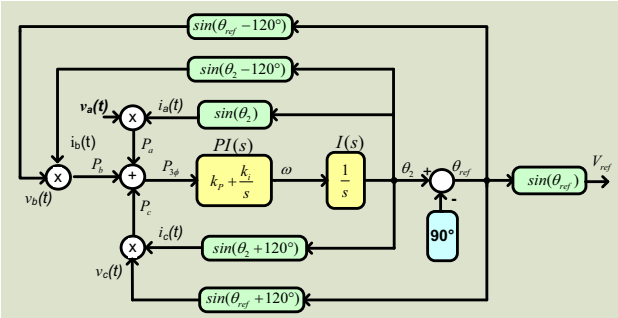

Figure 4. Single-phase PLL circuit.

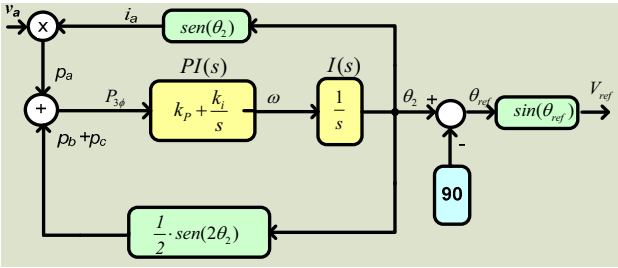

Figure 5. Single-phase PLL topology after simplification.

A. *Design of PI Controller and Simulation Results*

The PLL circuits could be obtained in the previous sessions considering that grid voltages are balanced and harmonic free. This ideal setup simplifies the design of the compensator, once that $p_{3\varphi}$ becomes null in steady state, and then it is only necessary to adjust gains k_p e k_i to obtain fast dynamic response.

However, grid voltages in practice have some harmonic content and may be unbalanced sometimes. This fact causes an alternating component to be added to $p_{3\varphi}$, which must be considered in the adjustment of the gains so that its effects are minimized and the frequency oscillation is within acceptable range to assure the adequate operation of PLL.

When the amplitude of voltage v_a varies, small 120-Hz ripple in $p_{3\varphi}$ results, therefore affecting frequency ω. Tradeoffs between the minimization of 120-Hz ripple and fast dynamic response must be made when adjusting the compensator gains. When highly distorted voltages exist, the resulting ripple frequency is higher than 120 Hz. Therefore, the design of a controller supposed to mitigate 120 Hz ripple will cause higher frequencies to be more attenuated.

From the aforementioned aspects, there comes a starting point to setup a PI controller. Expression (11) shows the open loop transfer function of the PLL system ($FTLA_{PLL}(s)$), expressions (12) and (13) represent the argument and phase for $\omega=\omega_c$, respectively, where ω_c is the crossing frequency.

$$FTLA_{PLL}(s) = \frac{k_i + k_p \cdot s}{s} \cdot \frac{1}{s} \tag{11}$$

$$\left| \frac{k_i + j \cdot k_p \cdot \omega_c}{(j \cdot \omega_c)^2} \right| = 1 \tag{12}$$

$$\angle \left(\frac{k_i + j \cdot k_p \cdot \omega_c}{(j \cdot \omega_c)^2} \right) = -(180^\circ - MF) \tag{13}$$

Where MF is the desired phase margin. Solving expressions (12) and (13) gives (14) and (15), where the arbitrary choice for the cut-off frequency and phase margin gives gains k_p and k_i.

$$\omega_c^4 - k_p^2 \cdot \omega_c^2 - k_i^2 = 0 \tag{14}$$

$$\frac{k_p \cdot \omega_c}{k_i} = \tan(MF) \tag{15}$$

After testing several values below 40 Hz for the crossing frequency, and by using simulation software PSIM, one has obtained k_p=116 and k_i=3500.

The open-loop transfer function of the system is then presented in (16), and the respective Bode diagrams are shown in Fig. 6.

$$FTLA_{PLL}(s) = \frac{3500 + 116 \cdot s}{s} \cdot \frac{1}{s} \tag{16}$$

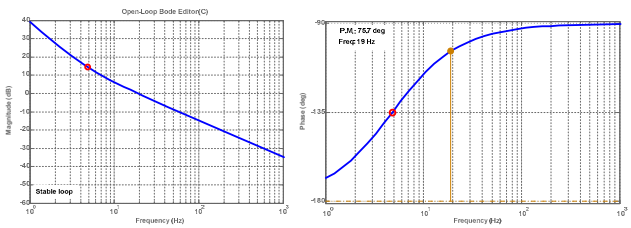

Figure 6. Bode diagram of transfer function $FTLA_{PLL}(s)$.

According to Fig. 6, the crossing frequency is 19 Hz. Calculating the argument for 120 Hz gives -16.24 dB, i.e. the attenuation is about 16 dB.

Simulation results of the proposed PLL with the PI controller set according to (16) are obtained using software PSIM and discussed as follows. Fig. 7 presents

voltage v_a, which is purely sinusoidal, as well as the reference signal. One can notice that the difference between the signals becomes negligible after 0.05 s, even though the system has not yet reached steady state, what occurs at 0.23 s, according to Fig. 8, where the frequency equals 377 rad/s.

A negative step of 20% is applied to voltage v_a at 300 ms in Fig. 9. One can notice that 120 Hz ripple results in $p_{3\varphi}$, although the reference signal waveform has not changed, as seen in the graph of θ_{ref}.

Therefore the attenuation of 16 dB is enough so that the ripple in $p_{3\varphi}$ does not affect the reference signal.

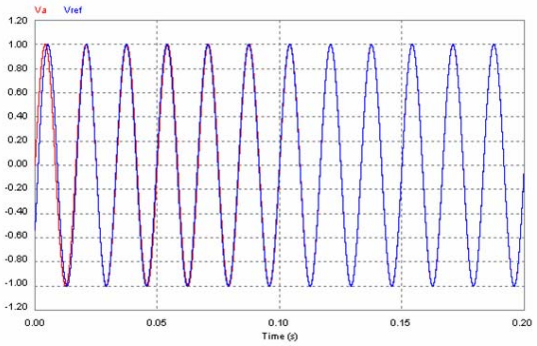

Figure 7. Voltage v_a (harmonic free) and reference signal.

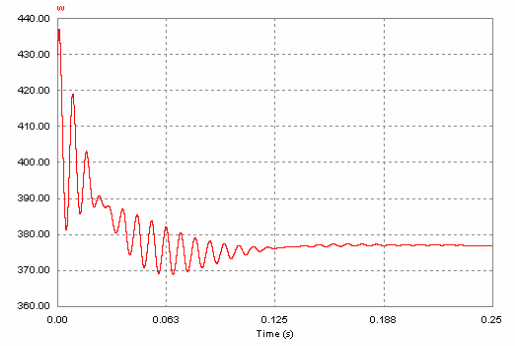

Figure 8. Behavior of frequency ω.

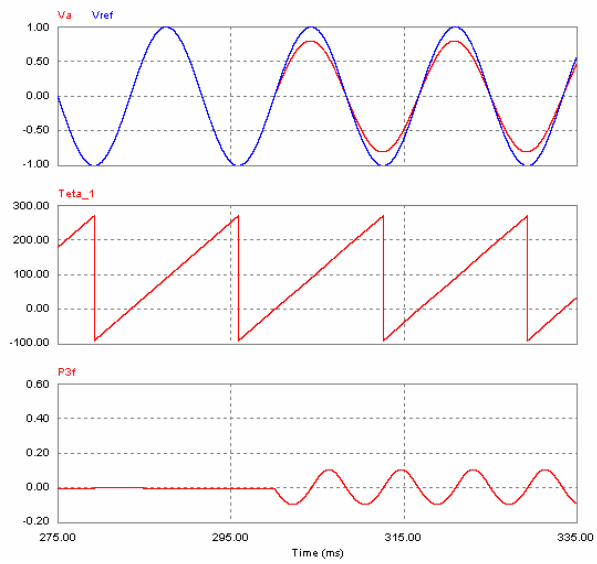

Figure 9. Negative voltage step of 20% applied to v_a.

Another test has been performed with highly distorted voltage applied to the PLL circuit. According to Fig. 11, the reference signal is sinusoidal and in phase with voltage v_a. Fig. 10 shows the presence of noise in $p_{3\varphi}$ due to the distortion of v_a. The noise can be attenuated using the PI controller as previously adjusted, which provides the signal shown in Fig. 11.

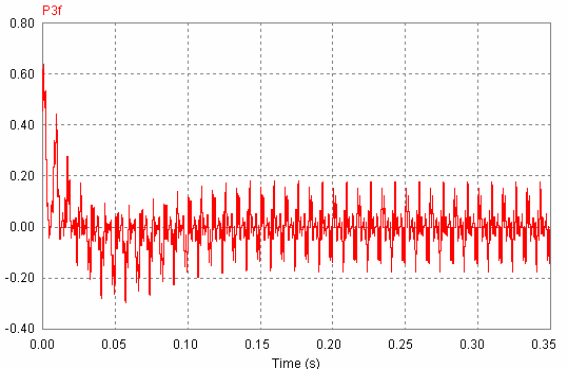

Figure 10. Signal $p_{3\varphi}$ with distorted voltage v_a.

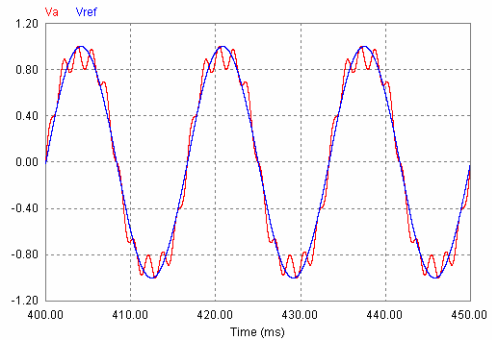

Figure 11. Reference signal with distorted voltage v_a.

The PI controller and the integrator in the z-domain could be obtained in z-domain using the Tustin discretization method known as bilinear approximation. This method consists in substituting parameter s for expression (17):

$$s = \frac{2}{T_a} \cdot \frac{(z-1)}{(z+1)} \tag{17}$$

Where T_a=1/f_a is the sampling frequency of the system. Thus the transfer functions in z-domain for the PI controller and the integrator are given by (18) and (19), respectively.

$$C_{PI\_PLL}(z) = 116 \cdot \frac{z-0.998}{z-1} \tag{18}$$

$$C_{I\_PLL}(z) = 0.000025 \times \frac{z+1}{z\text{-}1} \tag{19}$$

The expressions of the differences for the PI controller and the integrator to be implemented in the DSP to obtain the reference signal are given by (20) and (21), respectively.

$$u(k) = u(k-1) + 116 \cdot e_p(k) - 115.76 \cdot e_p(k-1) \tag{20}$$

$$u_i(k) = u_i(k-1) + 0.000025 \cdot e_i(k) + 0.000025 \cdot e_i(k-1) \tag{21}$$

IV. DIGITAL CONTROL SIMULATIONS

The DSP used in the ac line conditioner is TMS320LF2407A, manufactured by Texas Instruments. It is used to control the whole converter in order to obtain the signals for switches S_1 to S_8, besides generating the voltage reference, which is obtained through the PLL system. The control system implemented for the voltage conditioner in the DSP is shown in Fig. 12. The algorithm related to the DPLL system has signal $v_{a\text{-}DSP}$ as its input voltage, which is generated from the phase voltage v_a. This voltage, which must be attenuated as well as the remaining ones, has the commutation noise filtered and added to a continuous component in order to eliminate negative values. Signal v_a^* is applied to the DSP's analog-to-digital converter and has values between zero and 3.3 V. On the algorithm output, the reference voltage used in the control and the synchronizing voltage used to drive rectifier's switches S_1 to S_4 are presented. The compensating voltage of the average primary current regarding transformer T_1 is added to the sinusoidal reference generated by the PLL. Compensator $C_i(z)$ is used to eliminate any average values that current i_{Lo} may present. This compensator must have slow dynamic response so that it does not interfere with the operation of the output voltage (v_o) control loops. Thus, an integrator-type controller was implemented, with a crossover frequency around 1 Hz. Output voltage control is performed by two independent loops i.e. a feedfoward loop and another one with effective values. The first one aims to generate a control voltage that compensates variations and distortions existent in the input voltage (v_a) rapidly. This loop calculates the duty cycle (d) through system variables, isolating d in the static gain expression. A low-pass filter was also implemented tuned to a frequency of approximately 1 kHz. On the other hand, the second output voltage control loop has the purpose of minimizing the static error which may be present in v_o, correcting its effective value. This loop has a first order compensator tuned to a frequency two decades above the value for the current compensator. Figs. 13 to 15 show some simulation results of the system performance.

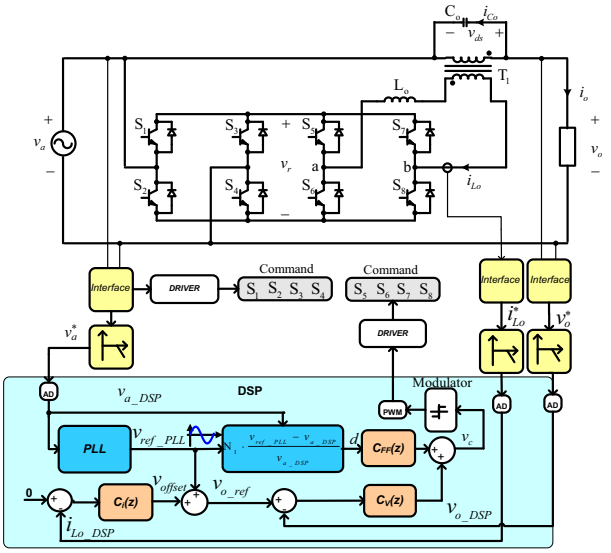

Figure 12. PLL simplified circuit.

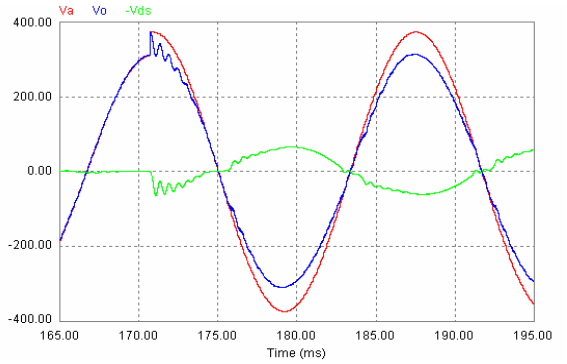

Figure 13. Input voltage transient due to +10% voltage step.

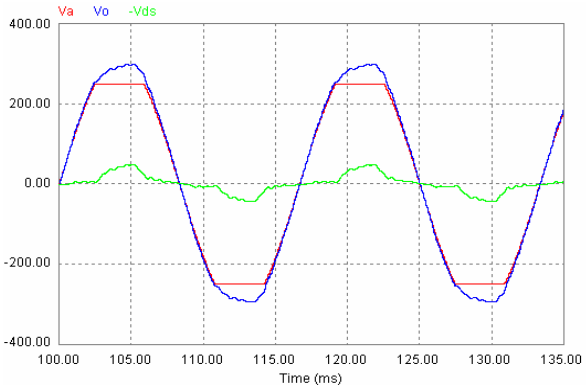

Figure 14. Load transient.

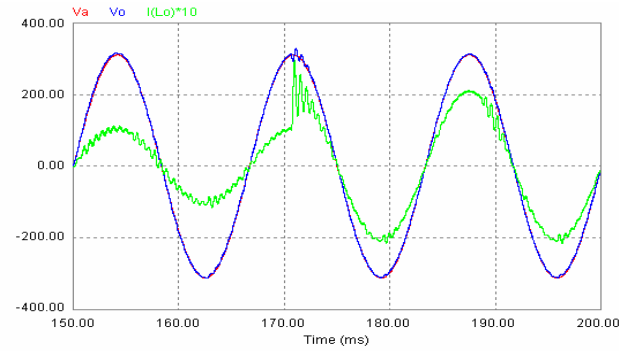

Figure 15. Disturbed input voltage.

V. EXPERIMENTAL RESULTS

The ac-ac conditioner built in the laboratory (Fig. 15) has the following specifications:

- $v_a = 220 \pm 20\%[V]$ - input voltage;
- $v_o = 220[V]$ - output voltage;
- $S_o = 3[kVA]$ - output power;
- $F_r = 60[Hz]$ - ac mains frequency;
- $F_s = 20[kHz]$ - switching frequency;
- $n_1 = 3$ - transformer T_1 ratio;
- $L_o = 570[\mu H], C_o = 120[\mu F]$ - output filter.

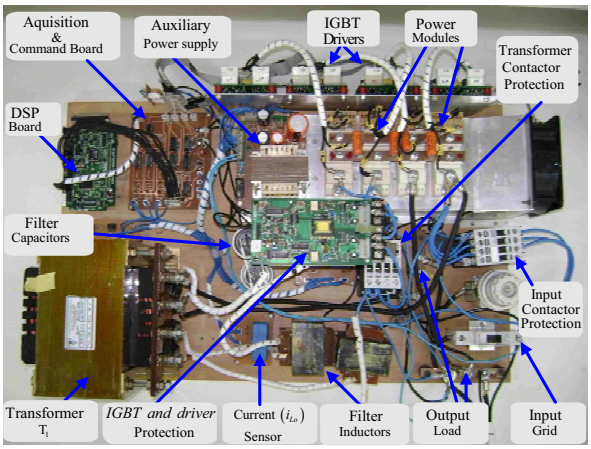

Figure 16. Conditioner built in the laboratory.

The waveforms regarding evaluation tests of the conditioner protection system is shown in Fig. 17. Overcurrent is applied to the conditioner in this test, which has responded satisfactorily.

The results regarding positive and negative input voltage steps are shown in Figs. 18 and 19, respectively. One can notice that the output voltage response is fast enough.

Fig. 20 presents some results on the operation with distorted input voltage. In this case, input voltage THD is 5%, although the obtained output voltage is nearly sinusoidal with THD equal to 3.2%. Therefore it has been demonstrated that the converter operates accurately as voltage regulator and series active filter using the proposed control loops.

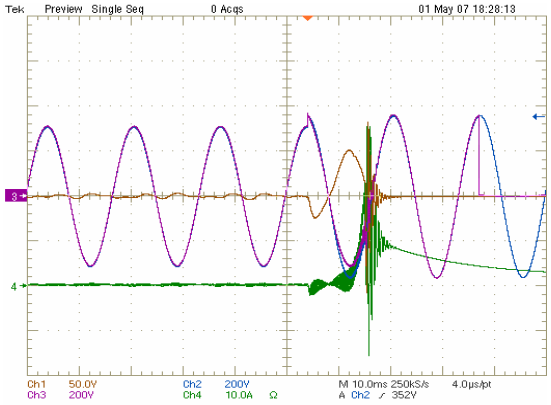

Figure 17. Test of overcurrent protection.

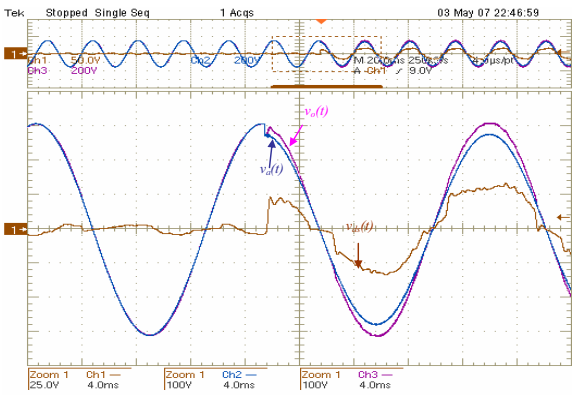

Figure 18. Input voltage transients: -10% input voltage.

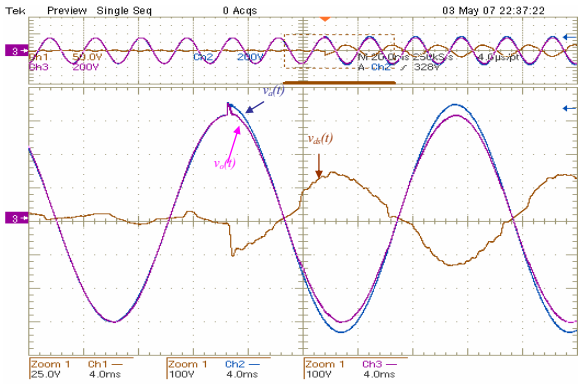

Figure 19. Input voltage transients: +10% input voltage.

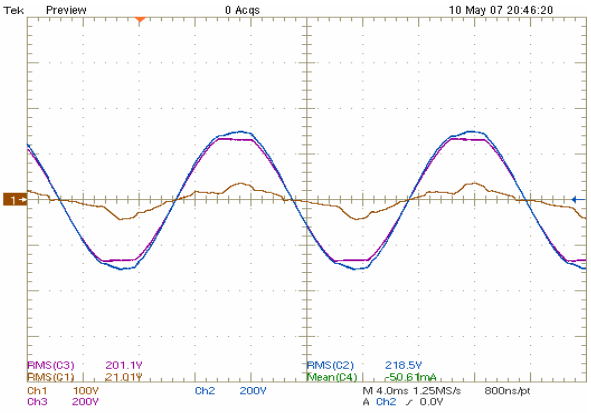

Figure 20. Input voltage disturbed in steady state conditions.

VI. CONCLUSIONS

This paper has presented a study on a digitally controlled 3-kVA ac line conditioner. The operating principles of the involved converters were described briefly. Details of the sinusoidal reference generation were also discussed. The use of DPLL in the digital implementation for sinusoidal reference and zero crossing detectors has provided very good results. The main output voltage control loops were designed, in the digital case with feedforward and effective v_o control loops. The implemented digital PLL has presented adequate performance, even when dealing with triangular waveforms, that is, high harmonic content. Experimental results show an appropriate behavior of the conditioner operating with distorted input voltage, and also under variations of load and input voltage. The control system of the output voltage, composed by the control loop of the rms value along with the feedforward loop reached the proposed goal, being capable to correct variations in amplitude that are within the compensation range, and also distortions in the waveform. The proposed conditioner demands the simultaneous existence of two control loops for the control of the output voltage. If the converter operates without the feedforward loop, it will not be able to correct distortions in the waveshape, operating as a simple stabilizer. In cases where it comes to operate without the control loop of the rms value, there will be differences in the rms value of the output voltage, being unable to eliminate this problem.

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