A Novel Converter Topology and its Application in Line Voltage Conditioner

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***Abstract* – This work presents the study of a new converter topology and its application in line voltage conditioner. In this paper it is studied the description of the operation, the operation modes, the modeling and the application of this new converter topology in line voltage conditioner. This conditioner supplies energy for linear and non-linear loads, providing stable output voltage and with smaller harmonic content, in relation to the input. At the end of this work the design and the experimental results of the voltage conditioner of 10kVA, with an output voltage of 220V and the switching frequency of 20kHz, are presented.**

I. INTRODUCTION

One of the techniques used to stabilize the load voltage is by the appropriate selection of derivations of transformers. This technique is efficient, as long as the number of derivations is large, what implicates in a great number of semiconductors. Phase control stabilizers do not allow elevate the output voltage, they only have voltage down capability. Lately most of the stabilizers used tiristor technology. Such converters, however, have slow answer and they need great input and output filters to attenuate the high order harmonics.

This work presents a new converter topology with PWM modulation which source and load positions can be changed, what modifies some characteristics of the circuit. The converter, according to the modulation, may have several applications, such as: supplying energy for continuous current machines operating in the four quadrants, cycleconverters and voltage conditioner. This last application was used for the experimental proof of the operation of the new converter topology proposed.

The voltage conditioners differ from the stabilizers, because besides stabilizing the output voltage they correct the harmonic content, working as active filters of voltage.

A recent study on line voltage conditioners is the topology studied in [2, 3]. This voltage conditioner operates with modulation PWM in high frequency (20kHz) and, for being the type of voltage compensator, it processes only part of the load power, increasing the total efficiency of the structure. The present work was inspired in this conditioner, in way to create a converter with two bi-directional switches in less, in other words, one branch less. However the conditioner in [2, 3] has the advantage of presenting a smaller isolation transformer in relation to the used in this work for the same load power.

II. PROPOSED CONVERTER

A. Presentation and Description of Converter

The new converter topology in study can operate with isolated input, as shown in Fig. 1, or isolated output, shown in Fig. 2. For this configuration change, ideally, it is enough to change the position of the input source with the load, besides modifying the commands of the bi-directional switches. However, in the practical implementation of the converter in voltage conditioners, the topology chosen was that with isolated input, for the fact that this topology does not need an extra control loop for the control of the offset voltage in the transformer input. Besides, the topology with isolated input, applied in voltage conditioners, allows the instantaneous opening of the switches in case of a short circuit in the load.

The principle of the operation of the two topologies is the same. So, from this part of the paper on we will study only the topology with isolated input and its application in conditioner of alternate voltage.

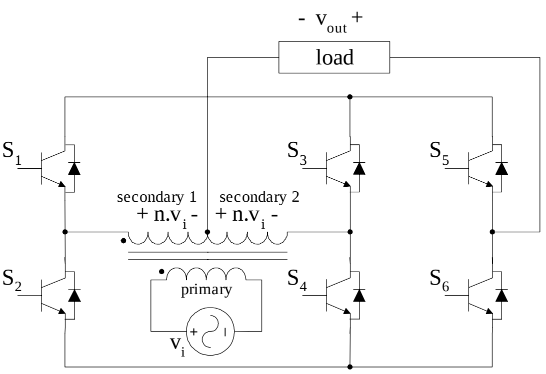

Fig. 1. Isolated input converter.

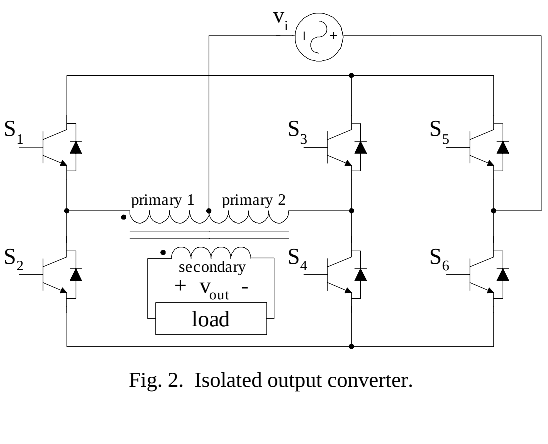

Fig. 2. Isolated output converter.

B. Converter Operation Modes

First Case – Positive input voltage (switches S_1 and S_4 enabled while S_2 and S_3 are blocked).

1st mode – In this operation mode the switch S_5 is enabled and S_6 is blocked. Therefore, if the load current I_o goes larger than zero then the switches D_1 and S_5 lead, otherwise I_o circulates through S_1 and D_5, as it is represented in Fig. 3.

2nd mode – Now the switch S_5 is blocked and S_6 is enabled. Therefore, if $I_o > 0$ then the load current circulates through S_4 and D_6, otherwise it is leaded by D_4 and S_6, as it is shown in Fig. 4.

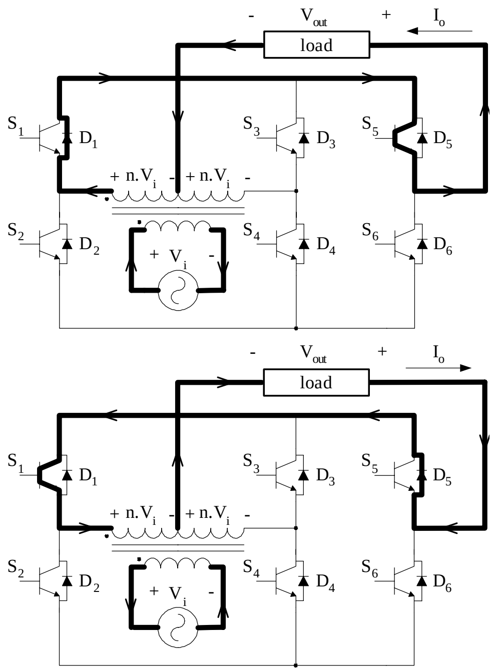

Fig. 3. First operation mode.

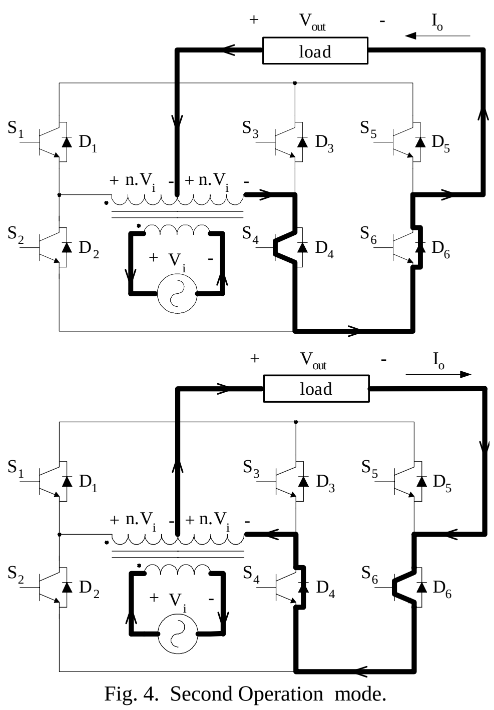

Fig. 4. Second Operation mode.

Second Case – Negative input voltage (switches S_2 and S_3 are enabled while S_1 and S_4 are blocked).

3rd mode – In this operation mode the switch S_5 is enabled, while the switch S_6 is blocked. In this way, if $I_o > 0$, then the load current circulates through D_3 and S_5, otherwise the switches S_3 and D_5 lead, as Fig. 5 illustrates.

4th mode – In this situation the switch S_5 is enabled and S_6 is blocked. Therefore, if $I_o > 0$, then I_o circulates through S_2 and D_6, otherwise the load current circulates through D_2 and S_6, as it is represented in Fig. 6.

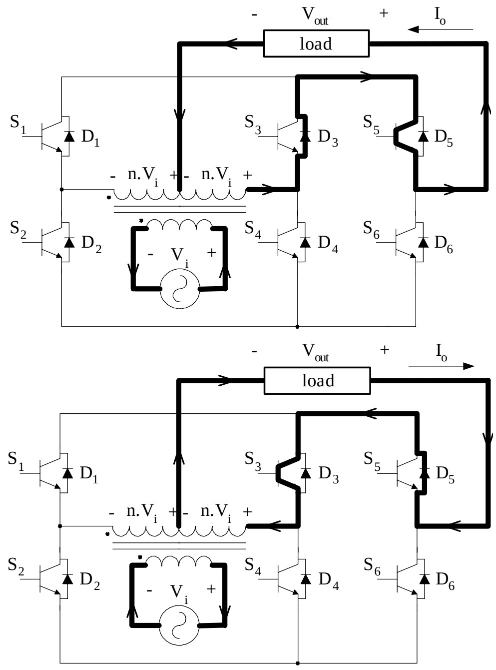

Fig. 5. Third operation mode.

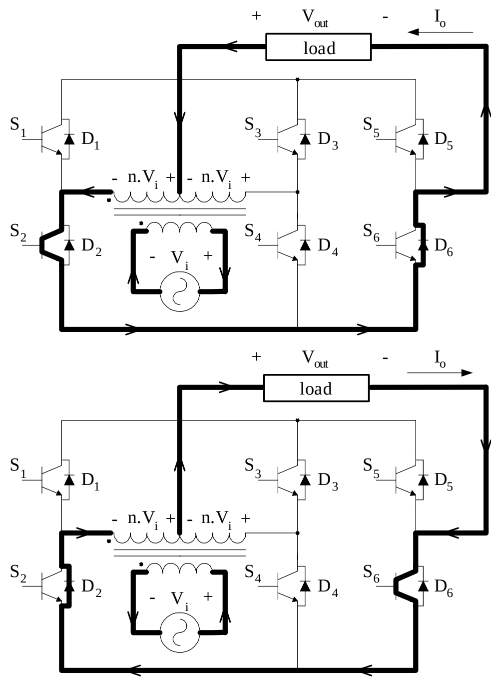

Fig. 6. Fourth operation mode.

C. *Simplification of the Rectifier Part*

To facilitate the understanding of the converter operation we can simplify the rectifier part and redraw the converter with isolated input according to Fig. 7. However, the command of the switches that operate in high frequency depends on the application that is being destined the converter.

In applications with output voltage in the same frequency of the main, the control voltage for the modulation is synchronized with the input voltage. Therefore, during the positive semicycle of the main voltage, the switch S_5 operates with duty cycle D and the switch S_6 commutes with duty cycle (1-D). In the negative semicycle of the main voltage the duty cycle is inverted, the switch S_5 operates with duty cycle (1-D) and the switch S_6 operates with duty cycle D.

For applications in supply of continuous current machines the duty cycle doesn't change for the positive and negative main semicycles, except when there is a change of polarity of the output voltage.

When the converter is applied to cycleconverters, the duty cycle of the switches S_5 and S_6 is constant in a certain number of semicycles and it inverts during the same number of semicycles. Thus the fundamental frequency of the output voltage is smaller in relation to the input frequency.

D. *Modulation*

The modulation of the converter is accomplished with a rectangular control voltage, according to Fig. 8, different from the traditional sinusoidal modulation that has the control voltage in the form of a sinusoid.

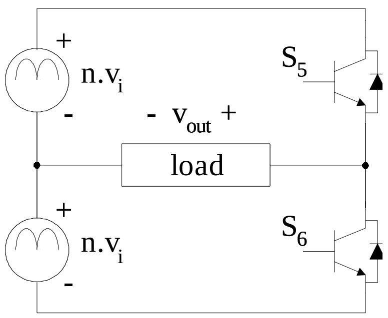

Fig. 7. Simplified circuit for the isolated input converter.

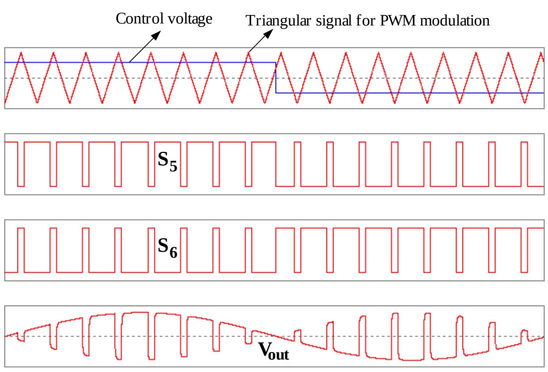

Fig. 8. Output voltage for modulation at two levels.

E. *Static Transfer Characteristic*

It is observed starting from Fig. 8 that by doing the integral of the output voltage in a switching period we can find the instantaneous medium value of the output voltage of the converter. Therefore, the characteristic of static transfer of the converter modulated at two levels is given by the equation (1).

$$\boxed{\overline{V_{out}} = (2D-1)nV_i} \tag{1}$$

III. VOLTAGE CONDITIONER

A. *Conditioner Circuit and Operation Description*

The voltage conditioner shown in Fig. 9 uses the converter proposed with isolated input and a filter L_oC_o in the output of this converter. So, this output filter is connected in series with the main and the load so as to compensate the voltage in the load for a variation of the input voltage.

Analyzing the operation modes, it is verified that the current of the filtering inductor is commuted in high frequency from a secondary winding to another. These abrupt changes of current in the dispersion inductances of secondary windings (L_{d1} and L_{d2}) would cause a voltage peak, which would damage the switches and the operation of the voltage conditioner. For this reason an uncoupling capacitor (C_{d1} and C_{d2}) are placed in parallel with each secondary winding.

B. *Modelling*

The static model is obtained starting from the converter static transfer characteristic. Then, adding the equation (1) with the voltage of the main, it is obtained:

$$\overline{V_o} = V_i + (2D-1)nV_i \Rightarrow \boxed{\overline{V_o} = V_i\left[1+n(2D-1)\right]} \tag{2}$$

The dynamic model of the voltage conditioner is obtained by considering the small signals model. In this model it can be considered the low frequency sources of alternate voltage such as DC sources.

By using the model of the PWM switch of Vorpérian [4] in the continuous mode of current, the Fig. 9 can be redrawn according to Fig. 10.

Analyzing the circuit of Fig. 9 in permanent regime (s = 0) the values of I_x and V_x are calculated.

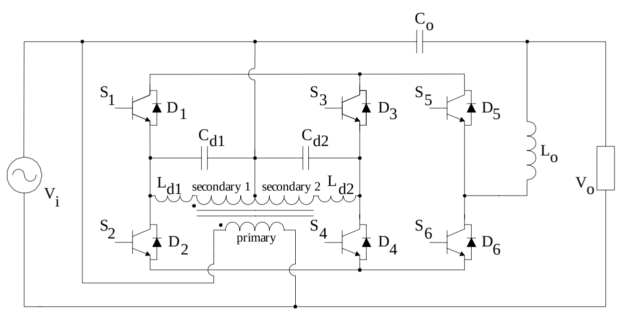

Fig. 9. Circuit of the line voltage conditioner.

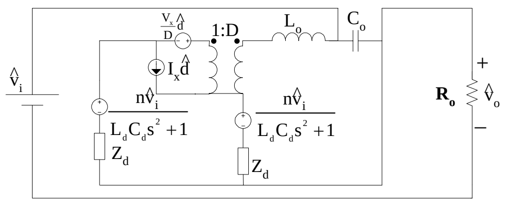

Fig. 10. Small signal model of the voltage conditioner.

So:

$$V_x = 2nV_i \tag{3}$$

$$I_x = \frac{V_i}{R_o}\left[n(2D-1)+1\right] \tag{4}$$

By making $\hat{v}_i = 0$ and analyzing the circuit of Fig. 10 it is found $\hat{v}_o(s)/\hat{d}(s)$.

$$\boxed{\frac{\hat{v}_o(s)}{\hat{d}(s)} = V_i\frac{2nR_o\left(L_dC_ds^2+1\right)+L_ds(1-2D)\left[n(2D-1)+1\right]}{(1+sC_oR_o)L_ds\left(2D^2-2D+1\right)+\left(s^2L_oC_oR_o+sL_o+R_o\right)\left(1+L_dC_ds^2\right)}} \tag{5}$$

By making $\hat{d} = 0$ and analyzing the circuit of Fig. 10 it is found $\hat{v}_o(s)/\hat{v}_i(s)$.

$$\boxed{\frac{\hat{v}_o(s)}{\hat{v}_i(s)} = R_o.\frac{n(2D-1)+L_dC_ds^2+1+L_dC_os^2\left(2D^2-2D+1\right)+L_oC_os^2\left(L_dC_ds^2+1\right)}{(sC_oR_o+1).L_ds.\left(2D^2-2D+1\right)+\left(s^2L_oC_oR_o+sL_o+R_o\right)\left(L_dC_ds^2+1\right)}} \tag{6}$$

IV. Voltage Conditioner Design

A. Design Specifications

For simulation and implementation of a prototype in laboratory, the following specifications of the voltage conditioner were used:

V_i = 311V ⇒ Amplitude of the input nominal voltage;
Δ = 0.2 ⇒ Variation of the input voltage (± 20%);
V_o = 311V ⇒ Amplitude of the output voltage;
P_o = 10 kW ⇒ Output nominal power;
ΔI_{Lo_Io} = 0.4 ⇒ Current variation in the inductor in relation to amplitude of the output current;
ΔV_{Co_Vo} = 0.03 ⇒ Variation of the capacitor voltage in relation to V_o;
f_s = 20 kHz ⇒ Commutation frequency.

B. Relation of the Transformer

Starting from the limits of variation of the input voltage of the voltage conditioner, the following transformation relations are obtained:

$V_{i\_max} = (1 + \Delta).V_i = 373.2$ V ⇒ D = 0 ⇒ n = 0.167
$V_{i\_min} = (1 - \Delta).V_i = 248.8$ V ⇒ D = 1 ⇒ n = 0.25

So, considering a sinusoidal input voltage and not considering the voltage drop, to satisfy the two situations above, the relation should be n = 0.25. However, due to the distortion of the input voltage and the voltage drop in the inductor L_o, the transformation relationship chosen was n = 0.5.

C. Uncoupling Capacitors

The uncoupling capacitors (C_d) were designed starting from the following specifications:

L_d = 50 μH ⇒ Parasite leakage inductance;
f_s = 20 kHz ⇒ Switching frequency.
f_{od} ⇒ Frequency of resonance between L_d e C_d;

Knowing that the low pass filter L_dC_d, it attenuate approximately 40 dB per decade, to frequencies above f_{od}. Then to reduce the voltage ripple, caused by the switching, it must be used $f_{od} < f_s$.

$$f_{od} < f_s \Rightarrow \frac{1}{\sqrt{L_dC_d}} < 2\pi f_s \Rightarrow \boxed{C_d > \frac{1}{4\pi^2 f_s{}^2 L_d}} \Rightarrow C_d > 1.27\ \mu F$$

Choosing $f_{od} \approx f_s/4$ $\quad C_d = 20.3\ \mu F \Rightarrow \boxed{C_d = 20\mu F}$

D. Output filter

Starting from the relationship volt-ampere of the inductor it is found:

$$v_L = L\frac{di_L}{dt} \quad\Rightarrow\quad nV_i - V_{Co} = \frac{L_o\Delta I_{Lo}f_s}{D_o} \tag{7}$$

The maximum ripple happens for D_o = 0.5. Therefore:

$$\boxed{L_o = \frac{nV_i0.5}{\Delta I_{Lo}f_s}} \quad\Rightarrow\quad \boxed{L_o = 150\mu H} \tag{8}$$

Considering that all the current variation in the inductor will go by through the filtering capacitor, decomposing this current in series of Fourier and conserving the fundamental component, it is obtained:

$$i_{Co} = \frac{4\Delta I_{Lo}}{\pi^2}.\cos\omega t \tag{9}$$

By multiplying the current with the impedance of the capacitor:

$$v_{Co} = i_{Co}.X_{Co} = \frac{i_{Co}}{\omega C_o} \Rightarrow v_{Co} = \frac{4\Delta I_{Lo}}{2\pi^3 fC_o}.\cos\left(\omega t - \frac{\pi}{2}\right) \tag{10}$$

Then the amplitude of the alternated component of the voltage v_{Co} will be:

$$\frac{\Delta V_{Co}}{2} = \frac{2\Delta I_{Lo}}{\pi^3 C_o f} \tag{11}$$

So:

$$\boxed{C_o = \frac{4\Delta I_{Lo}}{\pi^3 f_s \Delta V_C}} \quad\Rightarrow\quad \boxed{C_o = 20\mu F} \tag{12}$$

E. Controller Design

It was used for the control of the plant a proportional integral derivative controller (PID), presented in Fig. 12, designed for the plant model of the equation (5).

The PID controller used in the voltage conditioner was designed for the worst case, when the current of the non-linear load arrives in zero to each semicycle, in other words, for $R_o = \infty$. For this reason, the controller's design is done for this situation. It is observed in the equation (5) that, by making $R_o = \infty$, all the poles and the zeros of the plant move into the imaginary axis.

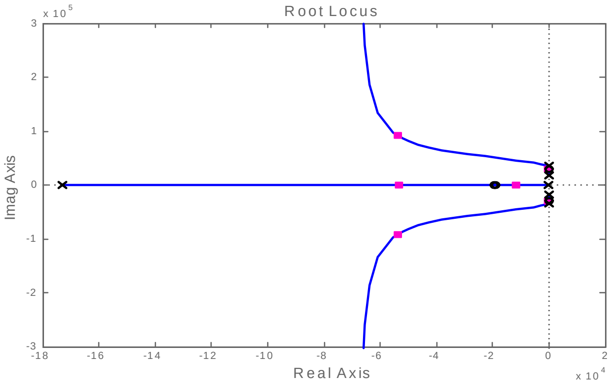

Fig. 11. Root locus of the plant with the controller.

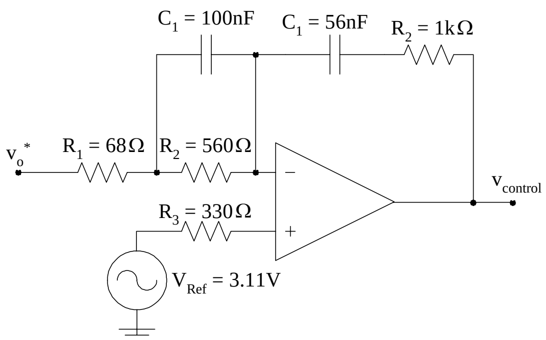

Fig. 12. Circuit of the PID compensator.

In the PID compensator design, a pole was placed in the origin so that the system should have null error to step in permanent regime, two zeros in the filter resonance frequency and a pole with the frequency nine times larger than the resonance frequency to improve the speed of the plant answer. The controller's gain was adjusted so that the plant presented the best possible dampening, by using a PID compensator. Thus, this gain was adjusted according to the root locus of the system into closed loop such as presented in Fig. 11. In the instant that the current of the non-linear load gets to zero, the system oscillates, therefore the concern with the dampening.

The equation (13) presents the PID controller transfer function, where:

$V_o^* = 0.01V_o.$

$$G_{control}(s)=\frac{v_{control}(s)}{v_o^*(s)}=\frac{[R_2C_1s+1].[R_4C_2s+1]}{C_2(R_1+R_2)s\left[\frac{C_1R_1R_2}{R_1+R_2}.s+1\right]} \qquad (13)$$

V. CONDITIONER EXPERIMENTAL RESULTS

A. *Analysis with Linear and Non-linear Load*

Fig. 13 and Fig. 14 show the analysis with resistive load for input voltage -14% of the nominal value and +14% of the nominal value, respectively.

It was verified in the analysis of resistive load, with nominal power and variation of the input voltage of -14% to +14% of the nominal value, that the output voltage is corrected in 220 V±0,5%.

Fig. 15 shows the analysis with non-linear load in the nominal power and with crest factor CF = 3.0.

In both analysis, with linear and non-linear load, the total harmonic distortion (THD) of the output voltage were below 5% and any harmonic component had not larger value than 3%, attending to the limits of THD of the norm IEEE 519/92 [1].

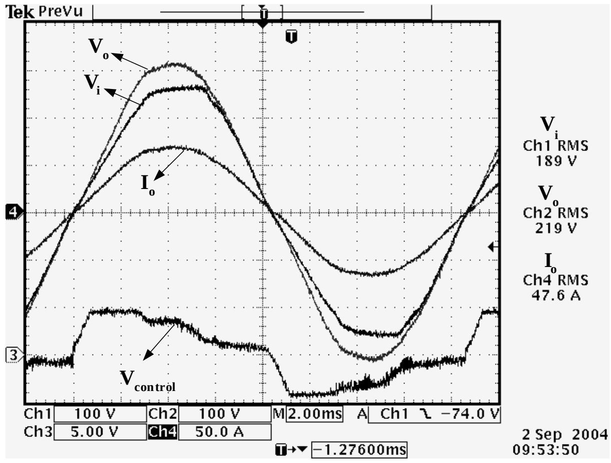

Fig. 13. v_i (-14%), v_o, $v_{control}$ and i_o for P_o = 10 kW.

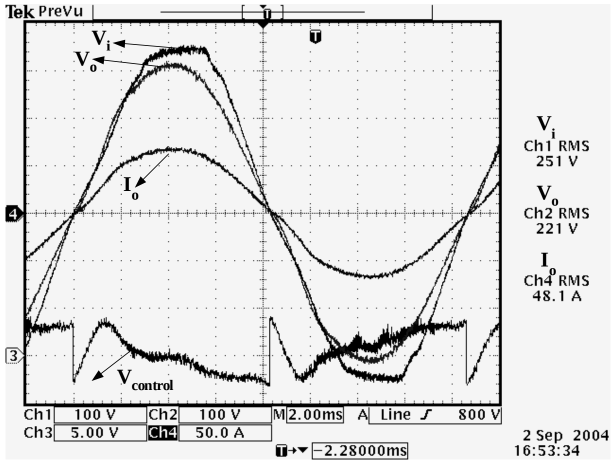

Fig. 14. v_i (+14%), v_o, $v_{control}$ and i_o for P_o = 10 kW.

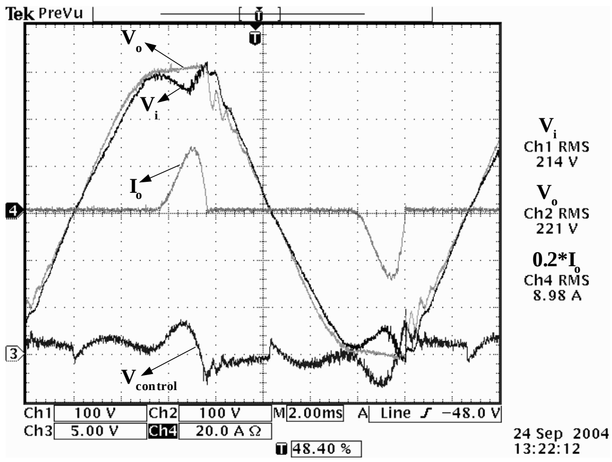

Fig. 15. v_i, v_o, $v_{control}$ and $0.2i_o$ for P_o = 10 kVA.

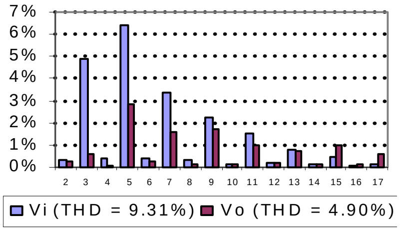

Fig. 16. Harmonics of v_i and v_o for non-linear load.

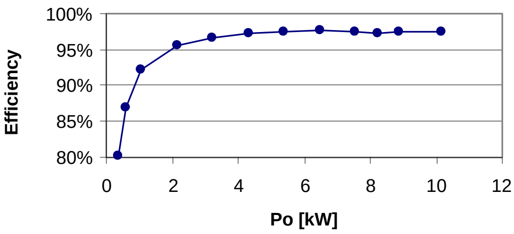

Fig. 17. Efficiency of the voltage conditioner.

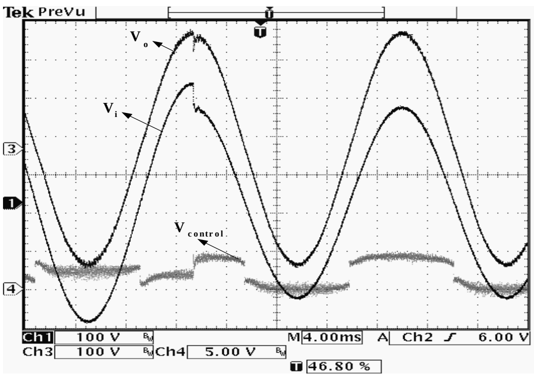

Fig. 18. Input voltage disturbance of -20%.

It is shown in Fig. 15 that the input voltage, given by main has a big falling during the conduction of the non-linear load. In this way, even with voltage near to nominal value in the input, the drop is of the order of almost 20%, what it is already the variation allowed by the design. If the same is operated with -20% in the input voltage, then during the conduction of the non-linear load this variation may get near to -40%, what is outside the designed range for the correction of the output voltage.

B. *Efficiency*

For the fact of the voltage conditioner process only part of the nominal power, the same presents a high efficiency.

The behavior of the voltage conditioner efficiency curve practically did not modify in all the range of the input voltage. The efficiency only varied in agreement with the load power, according to Fig. 17. In the nominal power the efficiency was around 97%.

C. *Disturbances in the input voltage and of the load*

Analyses were accomplished with instantaneous disturbances of input voltage, with variations of -20%, shown in Fig. 18, -10%, +20% and +10% of the nominal voltage, for the conditioner operating without load. For these situations the correction of the output voltage was practically instantaneous.

In the test of instantaneous increment of 50% of the load (0 to 5 kVA), the output voltage presents a small oscillation and it is stabilized in 1/8 of the period of the input voltage.

VI. Conclusions

It was accomplish in this work the study of a new converter topology. It was presented the theoretical study starting from the operation description, operation stages and modeling of the converter. Throughout these concepts, it was designed a voltage conditioner to feed linear and non-linear loads with power of 10 kVA.

An important commitment in the design of the voltage conditioner is with the transformation relationship, the range of the input voltage variation and the output voltage static error. If larger the secondary voltage, larger is the input voltage variation range that the conditioner can regulate with low static error. However, the whole load current goes by the transformer, what implicates in the power of the same to be directly related to the secondary voltage.

Besides the input voltage variation range, the deformation of the main voltage can to saturate the control voltage, demanding high voltage on the secondary winding to correct this distortion. Besides, for non-linear loads the current derived increase produces a fall of significant voltage in the filtering inductor.

For the fact of the conditioner process only part of the load power, the same presented an excellent efficiency, around 97%.

The voltage conditioner proposed presented practically instantaneous correction of the output voltage, face the load and input voltage variations, what avoids over-voltage and failure for the consumers.

For input voltage around ±15%, the output voltage RMS was corrected in 220 V±0,6%. During all the tests accomplished with the prototype the ripple in high frequency of the output voltage was around 3% and the output total harmonic distortion was always reduced in relation to the input. In this way, the presented converter presented is appropriate for implementation in line voltage conditioners.

By virtue of the independence between the phases, this design can be used in three-phase voltage conditioners of 30 kVA that have neutral.

VII. References

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